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Device quality low temperature gate oxide growth using electron cyclotron resonance plasma oxidation of silicon

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by

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ABSTRACT

According to Moore's Law, which has been true so far, transistors density on a chip area doubles every two years. This increase in number of transistors requires reduced device dimensions or to say scaling by a factor of ~0.7. As the device dimensions are shrinking, high temperature processes used in CMOS device fabrication, e.g. thermal oxidation of silicon to grow gate oxide, are becoming incompatible with CMOS processing. High temperature processes could change the impurity profile in Si, produce stresses on Si wafer, and also result in high thermal budget. In the past, many attempts have been made to reduce the oxidation temperature of Si by using high pressures of oxidizing gases, rapid thermal oxidation process, and plasma-assisted oxidation. In all these processes, plasma-assisted oxidation process, because of possible low processing temperatures, has gained considerable attention. However devices using plasma oxide have suffered with low oxidation rates, high interface defect density, plasma-induced damage and reliability issue.

This thesis presents the successful development of low temperature (~100^{o}C) silicon dioxide, which can be reliably used as a gate oxide in CMOS processing. Silicon dioxide was grown using an electron cyclotron resonance (ECR) plasma of oxygen/helium gaseous mixture. For the first time, MOSFET devices were fabricated using ECR plasma grown silicon dioxide as the gate oxide. Hot carrier induced (HCI) channel degradation of this gate oxide was studied and compared with thermally grown gate oxide. It was found that the high temperature annealing of ECR oxide improves channel resistance to HCI degradation.

In order to reduce the interface defect density and lower the processing temperature fluorine was added to the ECR plasma oxidation process. Small amount of fluorine gas in O_2/He plasma was found to enhance the oxidation rate significantly and lower the defect density by an order of magnitude. Most importantly, fluorine incorporated ECR oxide grown

at low temperature showed comparable HCI degradation as that of the thermal oxide with having to anneal it at high temperature.

MOS devices were fabricated to evaluate the oxide breakdown strength, interface defect density and oxide charges. Interface defect density (D_{it}), for ECR oxide grown using 10% O_2/He, was ~$1x10^{11}$ $cm^{-2}eV^{-1}$, while for thermal oxide D_{it} was ~$3x10^{10}$ $cm^{-2}eV^{-1}$. Defect density of the ECR oxide was significantly reduced by the inclusion of small amounts of fluorine during ECR plasma processing.

Plasma diagnosis was performed using optical emission spectroscopy (OES) and Langmuir probe. It was found that ECR plasma of pure oxygen gas has only O_2^+ ions and reactive oxygen (O^*) present in the plasma. Langmuir probe was used to study the plasma density and plasma sheath potential. Fourier Transform Infrared (FTIR) spectroscopy was used to identify the bonds in plasma grown silicon dioxide. X-ray Photoelectron Spectroscopy (XPS) was used to examine the chemical composition of the oxide.

The effect of temperature, pressure and DC bias on growth rate was studied. Higher densities of reactive species were observed at lower pressures. Plasma oxide growth showed very little dependence on the temperature. It was demonstrated that a positive bias significantly increases the growth rate and high negative biases halts the oxidation process. Results from these process parameters helped in understanding the oxide growth mechanism and are presented in the results section.

CHAPTER 1. INTRODUCTION

By and large crystalline Si is believed to be responsible for current CMOS technological success and advances made over the past several decades. However, many argue that it has become possible because of the magical properties of silicon dioxide, which is used as a gate dielectric in VLSI fabrication [1]. One of its most important properties is to make a low defect density interface with Si and also allow thinning of oxide as the device dimensions are scaled down to nanometer range. Therefore high quality ultra thin silicon dioxide is desired in semiconductor processing for ULSI. Conventionally silicon dioxide is grown at temperature above 1000^{o}C [2]. As the device dimensions are shrinking down, high temperature device processes operating at more than 1000^{o}C will tend to become incompatible with the device design [2]. High temperature process could change the doping profile of the impurities in the substrate. Also presence of high stresses, produced because of the different thermal expansion coefficients of Si and films present on it, could cause wafer bending, film cracking and defect formation in the underlying Si substrate. Thus low-temperature semiconductor device fabrication techniques are needed to prevent these problems. Lower temperature processes would also help in reducing the thermal budget of the processing and making the process more cost effective [2-8].

Several methods have been explored to reduce the processing temperature below 600^{o}C while maintaining a reasonable growth rate and a high quality gate oxide. These approaches include the use of high pressure, rapid thermal processing (RTP), silicon dioxide film deposition using plasma enhanced chemical vapor deposition (PECVD) and plasma-assisted oxidation of silicon [2]. Films deposited using PECVD show interfacial instability with large gap states generated by hydrogen atoms, which are included in the deposition process. This causes degradation in electrical properties and therefore PECVD oxide has failed to replace

the high quality thermal grown silicon dioxide. Owing to its low temperature processing, compared to RTP, plasma assisted oxidation has received much more attention.

In plasma assisted processes, researchers have tried DC, RF, microwave and high-density plasmas. DC and RF plasma suffer from high plasma potential causing high energy ions bombardment on Si wafer and contamination from the plasma reactor wall [8]. In all of the above methods, using microwave source based electron cyclotron resonance (ECR) plasma has drawn considerable attention [5]. It has high plasma density up to 10^{12} cm^{-3} at low pressures (0.1 to 50mT), lower ions energies (10-40 eV), and low and controllable plasma potential. This method not only yields a high oxidation rate, because of the high plasma density, but at the same time lower ions energies mean less damage and better oxide properties compared to other plasma sources [13].

Several groups have reported the electron cyclotron resonance (ECR) plasma assisted oxidation of silicon [8-20, 27]. Si wafers were successfully oxidized from room temperature to up to 640^{o}C using ECR plasma [8-20]. Oxide has been grown in a floating substrate and also with an applied external bias. Good electrical properties and improved growth rates have been reported when the substrate was positive biased [13]. Defect density and oxide breakdown strength has been reported to be in the range of $1.2x10^{10}$- $5x10^{11}$ $cm^{-2}eV^{-1}$ and 5-20 MV/cm respectively [12]. Chemical composition was studied using XPS and found to be fairly close to thermally grown silicon dioxide [9]. Actual growth mechanism still remains unknown; although many groups believe that it is because of the transport of O^{-} ions through the growing oxide layer, as suggested by the higher growth rates achieved when substrate was biased positively [12].

In order to qualify the ECR grown gate oxide process for ULSI fabrication, not only good electrical properties of gate oxide are required, but these properties must remain stable during device operation. Thus, gate oxide susceptibility to hot carrier induced degradation during

device operation is an important property to test. To our knowledge no other groups have reported the fabrication of MOSFET devices using ECR plasma oxide as a gate oxide.

In this project our objective was to grow a low temperature device quality gate oxide and study its reliability. Device quality gate oxides should exhibit the following properties [1]:

i. Uniform thickness across the wafer

ii. Low density of charges in the oxide and at the Si-SiO_2 interface

iii. High dielectric breakdown strength

iv. High resistance to hot-carriers induced damage

We systematically grew the gate oxide on p-type silicon wafers and studied the effects of processing conditions on electrical properties in MOS capacitors. Defect density and oxide breakdown strength were measured using MOS capacitors. NMOS transistor device parameters such as threshold voltage and mobility were measured. Reliability studies on NMOS devices were performed and compared with thermally grown dry-oxide as the gate oxide.

CHAPTER 2. LITERATURE REVIEW

Silicon dioxide is one of the most comprehensively studied dielectric, thanks to its magical properties in combination with Si and therefore used extensively in semiconductor industry [1]. Its has low interface defects with Si, possible growth mechanism on Si wafer, scalable with device dimensions, and good resistance to hot carrier induced degradation. Each of these fields has been explored in details. Even though we used ECR plasma, not high temperature furnaces, to grow the oxide, final properties requirements on oxide stay same. Oxide characterization techniques are not presented in this literature survey. We have briefly discussed the techniques we used in section 5. In this section we have mainly discussed the ECR plasma growth earlier done and important results.

Studies on ECR grown silicon dioxide have been done using different reactor designs, gaseous mixtures and growth conditions. Process parameters that were varied are mainly temperature, pressure, microwave power, gas flow rate and substrate bias. Plasma is characterized by its plasma density, electron temperature and plasma sheath potential. Most of the reactors were laboratory made and therefore plasma generated from these reactors differs. Final properties of the oxide are sensitive to a particular reactor design and therefore one has to be careful when comparing results reported elsewhere.

Below are some of the important results from the work done by several groups on ECR plasma oxidation of Si.

2.1 REACTOR DESIGN AND EXPERIMENTS

i. Kimura et. al. reported some of the very first work on silicon dioxide growth using ECR plasma of oxygen and studied the growth rate [8] Oxidation was performed under floating potential conditions at 0.2 mT chamber pressure and 600^{o}C substrate temperature. A schematic of the reactor used for this study is shown in Figure 2.1.1. Electrical properties were not reported. Infrared absorption and etch-rate measurements reveal that the physical properties of plasma oxidized SiO_2 at 600°C are structurally quite comparable to those of thermally oxidized SiO_2. Growth rate results were found to be different from what is expected by the Deal-Grove model for the thermal oxidation. Cabrera-Mott model, mainly used for metal oxide growth, was used to explain the growth results. Based upon this model the drift motion of oxygen ions across the oxide film under the influence of self-bias in the plasma is considered to be the plasma oxidation mechanism.

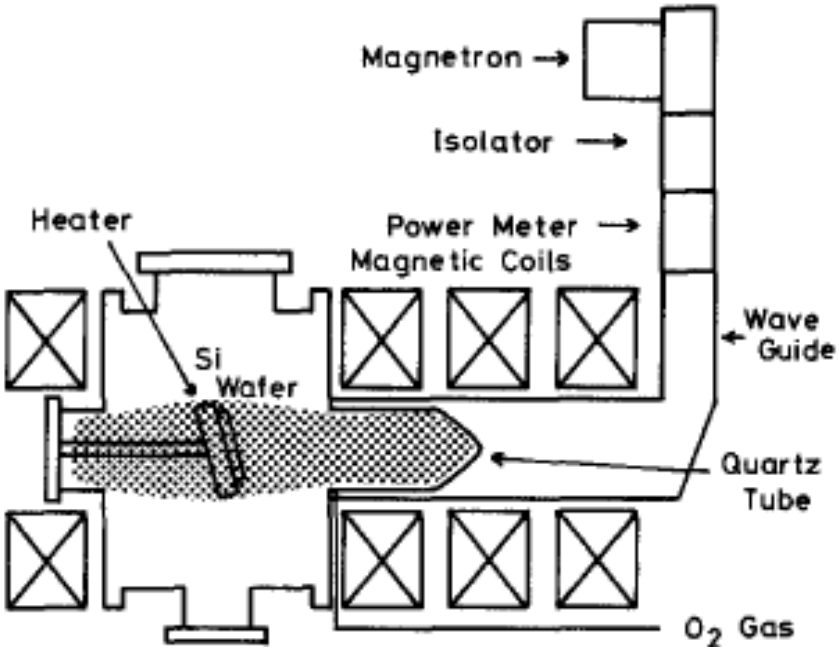


Figure 2.1.1: Schematic diagram of microwave plasma reactor [8]

ii. Plasma oxidation kinetics with no external bias on the substrate were analyzed by Kim et. al. [12]. Oxidation rate was studied for different chamber pressures, microwave power and substrate temperatures. They used microwave source of 50-1000W, 2.45 GHz and ECR source region was surrounded by the magnetic solenoids to get the resonance conditions (Figure 2.1.2). At microwave frequency of ω = 2.45 GHz, one needs B = 875 G to resonate the electron with the electron cyclotron frequency of $\omega_c = eB / m_e$ [1]. Pure oxygen gas (99.99%) was introduced through showerhead, placed 7.5 cm away from the stainless steel substrate holder. The substrate holder was self biased at –12 V during processing due to the ECR plasma induced sheath potential. Wafers were RCA cleaned and to remove any native oxide present at the surface wafers were dipped in HF solution, followed by water rinsing. However it was reported that in spite of chemical cleaning 10 Å of native oxide still existed.

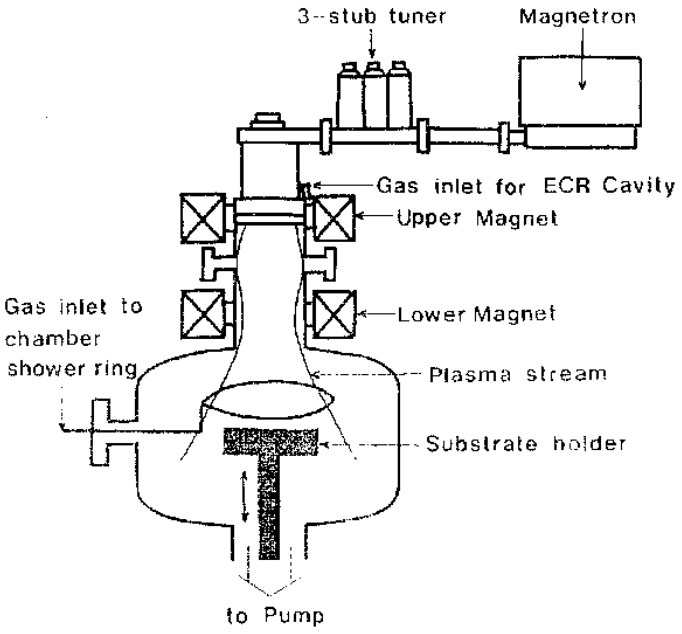


Figure 2.1 2: Schematic of the divergent magnetic field-type ECR source [12]

iii. Sung and Pang [14] used the ECR plasma reactor with 12 permanent magnets with the capability of varying distance between the source and sample. Substrate holder was water-cooled. Reactor had 12 permanents magnets to further confine the plasma and to reduce the longitudinal force. A microwave source of 200-1000 W was used for this experiment (Figure 2.1.3).

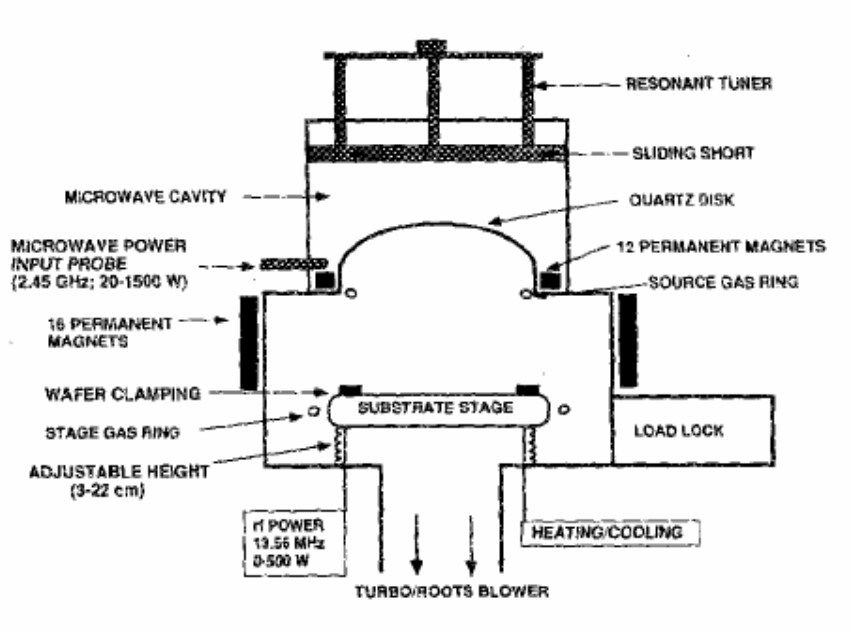


Figure 2.1 3: Schematic diagram of ECR reactor used with RF powered electrode [14]

vi. Salbert et al used a microwave plasma disk reactor (MPDR) to provide the uniform growth of silicon dioxide across the 3-inch Si wafer [10]. Experiments were done using 2.45 GHz frequency microwave at 280 W of power in a reactor designed with 16 permanent magnets of samarium-cobalt. Plasma was operated at 3 mT pressure with 10 sccm flow rate of 99.997% oxygen. Stainless steel substrate holder was not heated and self-heating of

wafer/substrate from the plasma considered to be ~200^{o}C. In all the experiments conducting wafer holder was subjected to 30, 40 or 50 V of anodic bias. Oxide thickness was measured as function of downstream plasma.

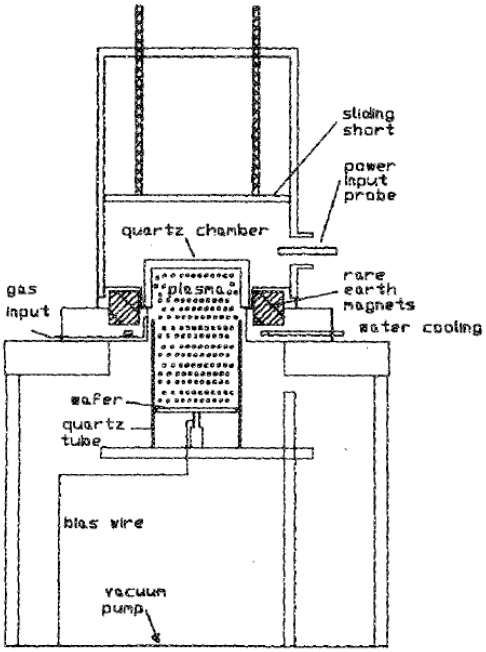


Figure 2.1 4: Cross-sectional view of ECR microwave cavity oxidation plasma system [10]

Carl, Hess and Lieberman [11] oxidized the single crystalline Si using ECR plasma reactor shown in Figure 2.1.5. They used a 2.45 GHz, 800 W microwave supply with matching network connected by a WR284 rectangular waveguide through a quartz window. Distance of Al substrate holder from the source chamber was ~14 cm. To aid the tuning optimization and monitor the plasma condition, Plasma Therm PSS-2 was used. This uses the optical emission of characteristics peaks from the plasma. Plasma density and electron temperature was determined using Langmuir probe.

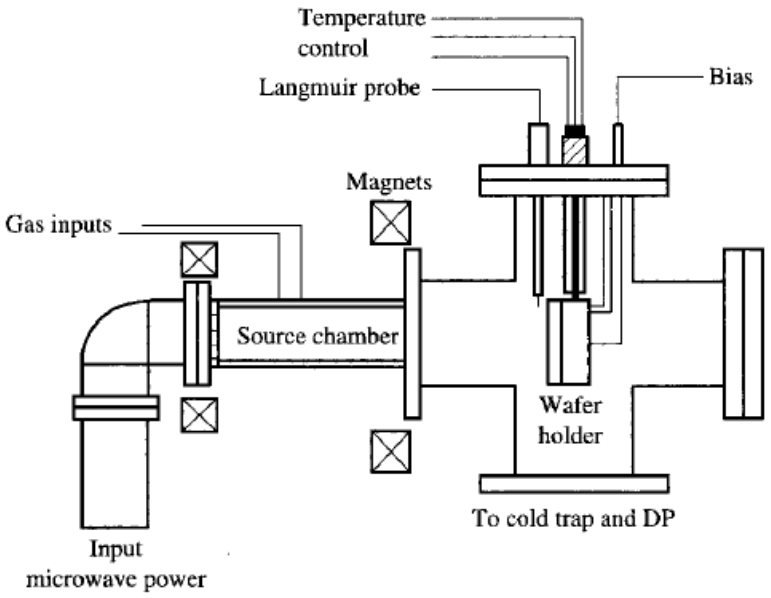


Figure 2.1.5: Schematic diagram of ECR reactor used [11]

2.2 GROWTH RESULTS

2.2.1 Effect of Temperature

Study from Kim [12] found increase in oxidation rate for temperatures above 350^{o}C. Oxidation rate decreased slightly for temperatures below 350^{o}C (Figure 2.2.1.1). It was believed that below 350^{o}C the neutral oxygen atom simultaneously diffused through the oxide layer, while at temperatures above 350^{o}C oxygen atom is thermalized and diffusion is thermally enhanced.

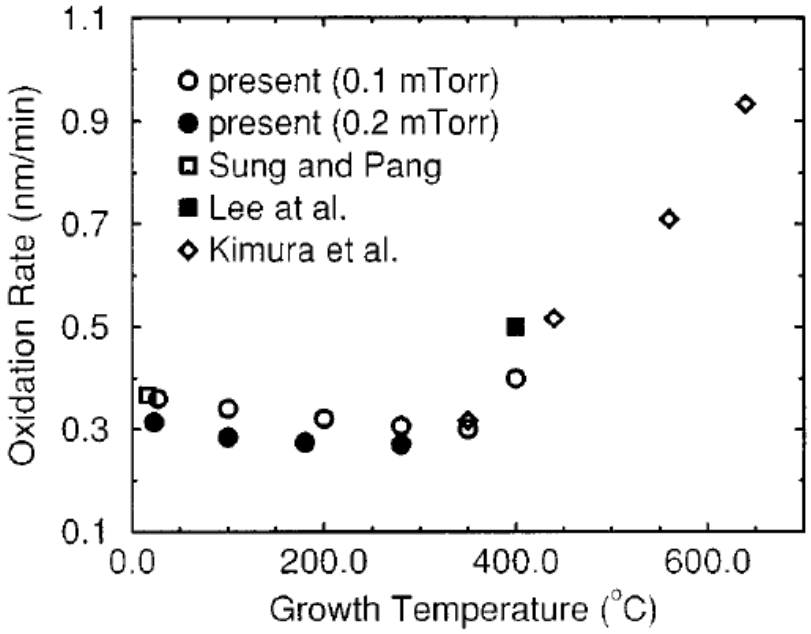


Figure 2.2.1 1: Temperature dependence on oxide thickness grown at 1000 W microwave power for 30 min [12]

Growth studies and electrical properties were studied by Kunio et al . Oxide was grown with a 2.45 GHz microwave source and a 500 W divergent magnetic field ECR plasma [22]. Chamber pressure was in 0.75 mT - 0.075 mT (10^{-1}-10^{-2} Pa) in an Ar/O_2 (20 sccm and 8 sccm) mixture. Study of temperature dependence on oxide growth rate found small

activation energy of only 0.02 eV for the initial oxide growth stages (Figure 2.1.1.2). It suggests that the film growth is not limited by the diffusion of oxidizing species through the oxide layer. Ion irradiation was thought to be the reason for such low activation energy.

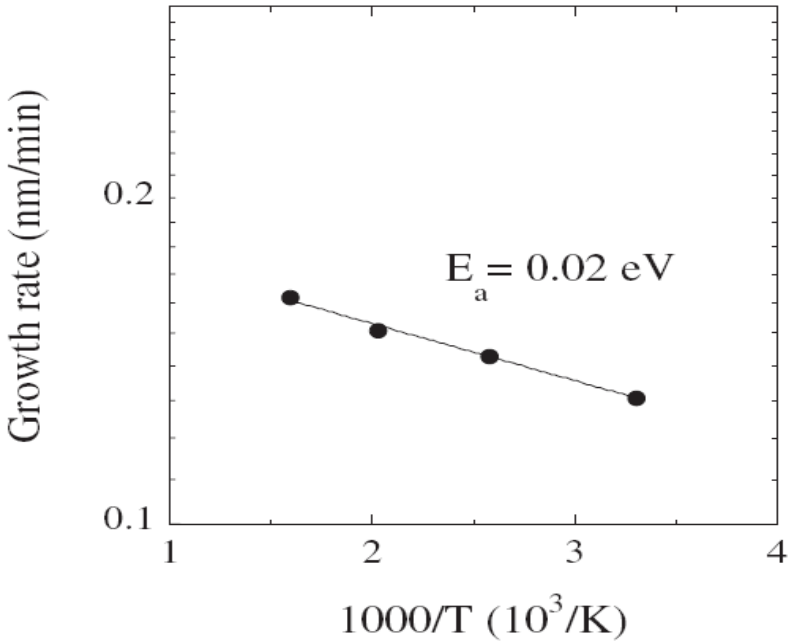


Figure 2.2.1 2: Arrhenius plot of growth rate showing small activation energy [22]

2.2.2 Effect of Pressure

Oxidation rate was found to decrease with the increase in pressure because of the decrease in plasma density at higher pressures (Figure 2.2.2.1) [12]. In this experiment oxidation rate also decreased at very low pressures because of the increase in O_2^+ ion peak intensity compared to reactive oxygen. At much lower pressure, preferential ionization of oxygen occurs than dissociation to generate reactive oxygen. Plasma intensities were measured using optical emission spectroscopy. Higher oxide growth rates were consistent with the maximum intensity of oxidizing species, which were assumed to be reactive oxygen.

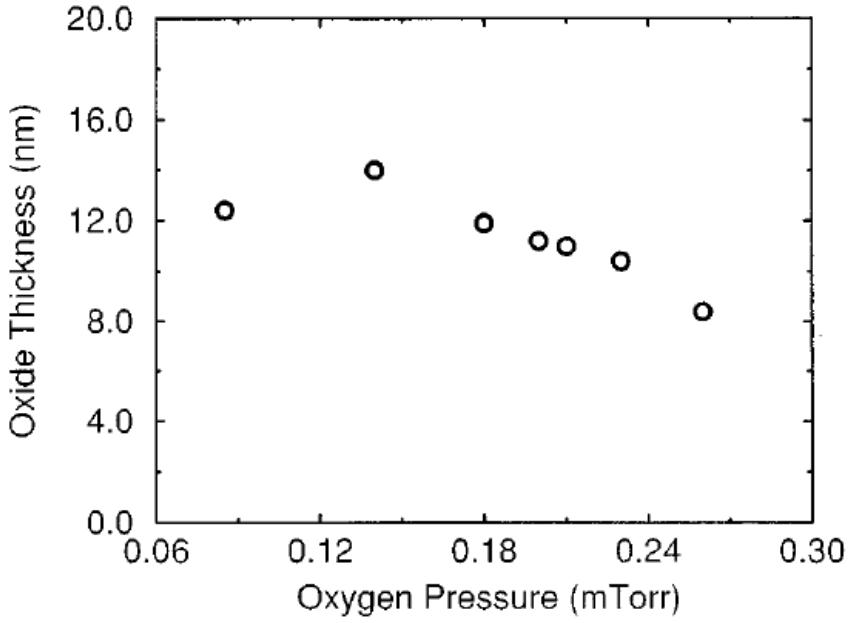


Figure 2.2.2 1: Oxygen pressure dependence on oxide thickness grown at room temperature for 30 min at 1000 W microwave power 10 sccm flow rate and 0.1 mT chamber pressure [12]

Experiments by Sung [15] showed that for pressure range of 5-50 mT there was no measurable change in the oxide thickness. But at lower pressures (0.25 mT), oxide thickness tripled (Figure 2.2.2.2). Pressure could change the dissociation efficiency, recombination rate and density of oxidizing radicals. At low pressures higher dissociation and lesser

recombination is expected and thus more reactive species are available for the oxidation process. Higher availability of oxidizing species was thought to be responsible for high oxidation rates.

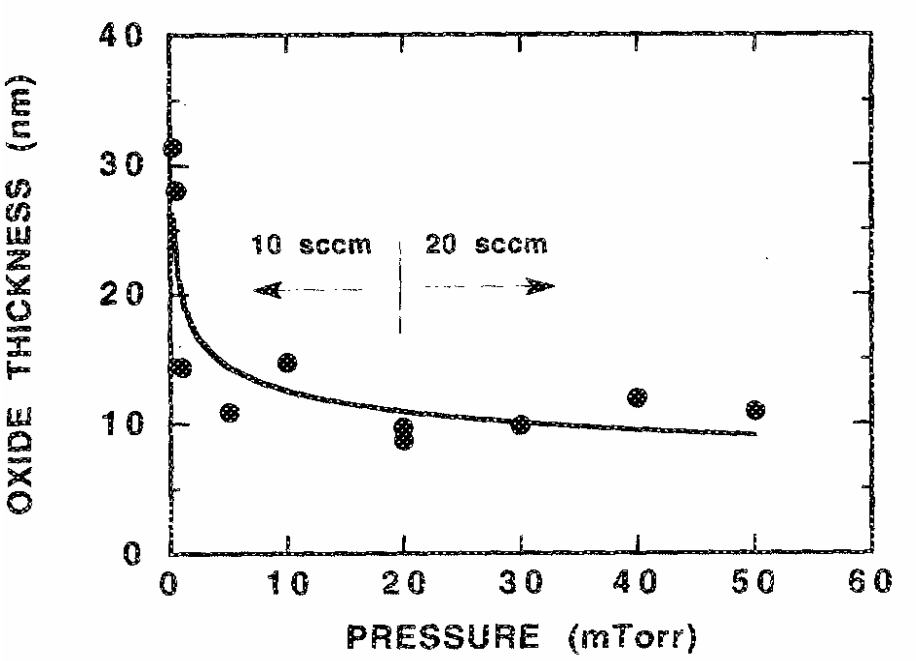


Figure 2.2.2 2: Dependence of oxide thickness on chamber pressure. The microwave power was 1000 W at 10 sccm of O_2 flow for 100 min with source to sample distance as 3 cm [15]

2.2.3 Effect of Power

Sung et al. [15] show an almost linear increase in growth rate with the microwave power (Figure 2.2.3.1). Kim et al. also obtained similar results (see Figure 2.2.3.2). Langmuir probe data showed an increase in ion densities with increase in microwave power. Ion density related increase in growth rate at room temperature indicate that the growth rate is not dependent on thermal energy. Plasma generated species could provide the good growth rates even at low temperatures. The O_2 flow was 10 sccm at 1 mT pressure for 100 min and the plasma source to sample distance was 3 cm.

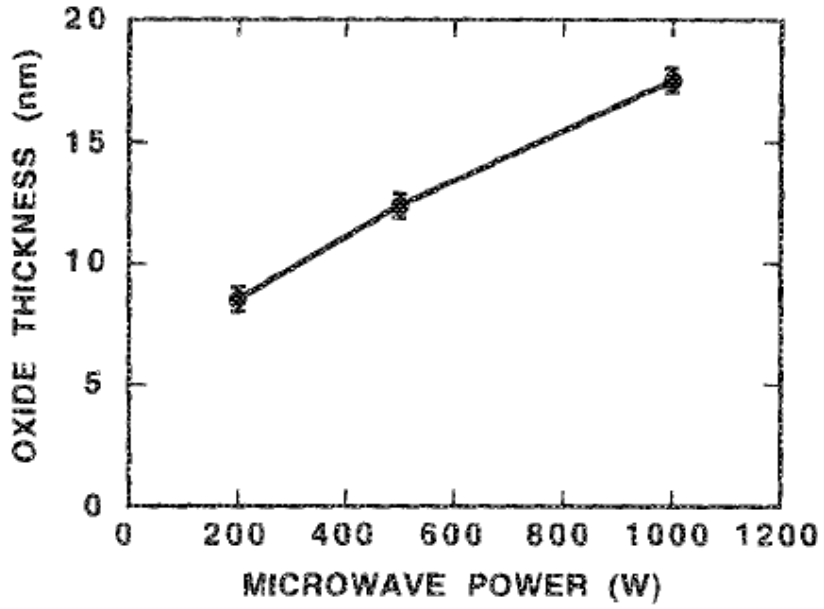


Figure 2.2.3 1: Dependence of oxide growth rate on microwave power [15]

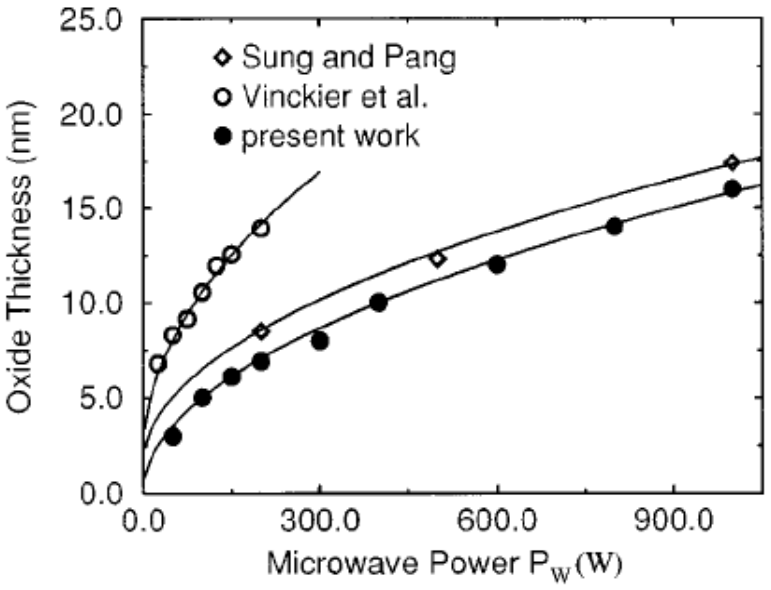


Figure 2.2.3.2: Microwave power dependence on oxide thickness grown at 0.1 mT of pressure for 30 min. As the power is increased, oxidation thickness parabolically increases implying the direct impact of the O atoms momentum [12]

2.2.4 Effect of Wafer Distance from Plasma Source

Salbert [10] and Sung [15] studied the oxide growth rate dependence as a function of distance from the source. Both of them found oxidation rate increased as the sample was moved closer to the source region and vice versa (see Figures 2.4.1 and 2.4.2). Reduction in oxide thickness with an increase in source to sample distance is related to less confinement at higher distances and implies a decrease in ion flux and a longer time for reactive species to recombine.

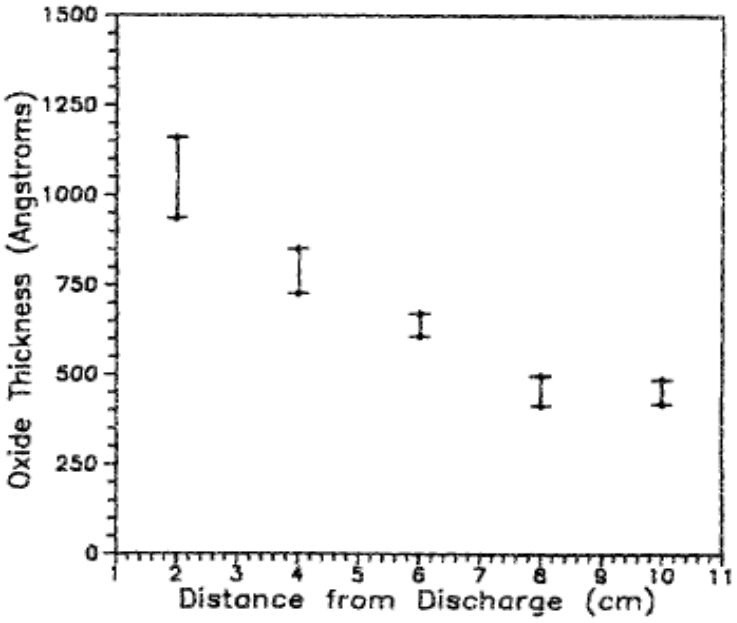


Figure 2.2.4.1: Oxide thickness as a function of downstream distance for 2 h growth with 280 W input power, 3 mT pressure and 40 V bias [10]

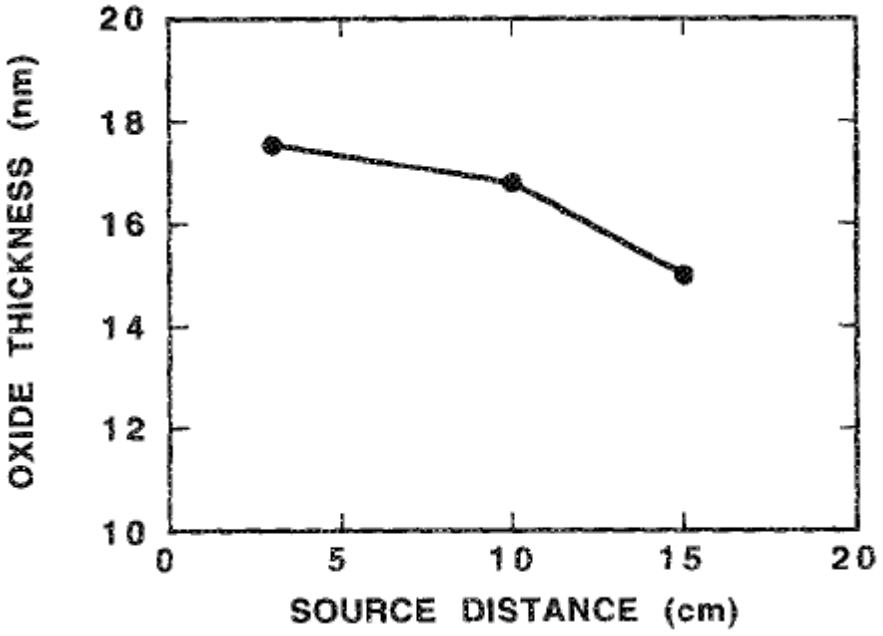


Figure 2.2.4 2: Oxide thickness as a function of downstream distance [15]

2.3 ELECTRICAL PROPERTIES

Salbert et al. fabricated MOS capacitors consisting of ~280 Å thick oxide films to study the oxide's electrical properties [10]. Films were formed on a p-type wafer using 3 mT of pressure with +40 DC bias applied to the substrate. Wafers were not heated and the temperature after the oxidation reached to ~200^{o}C. Oxide breakdown strength was reported to be ~7.6 MV/cm and fixed oxide charges were reported as $5x10^{11}$ cm^{-2}. Defect density (D_{it}) was found to be $5x10^{11}$ $eV^{-1}cm^{-2}$ (Figure 2.3.1). Defect density was measured using the slope of the experimental C-V graph and compared with the theoretical C-V curve, assuming fixed charge as $5x10^{11}$ cm-2 (Terman Method [39]). These values of defect densities are not only higher than the thermally annealed oxide but also higher than the ECR oxide defect density reported elsewhere.

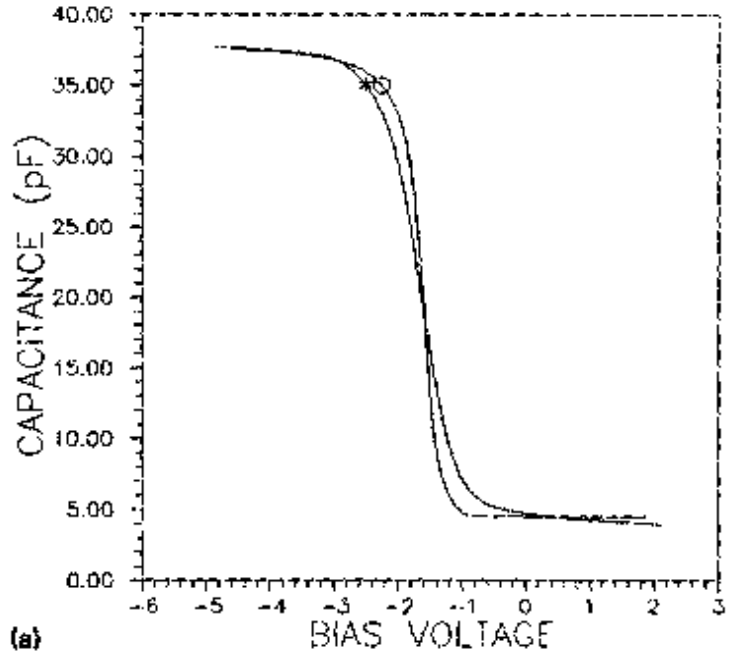


Figure 2.3 1: Theoretical (o) and measured (*) C-V curves. Theoretical curve assumes D_{it} =0 and Q_f = $5x10^{11}$ cm^{-3}. Stretch in measured curve used to calculate the defect density [10]

MOS capacitors of ~70 Å (area ~80 μm) oxide thickness were formed using Al as the gate metal [12]. Post metallization annealing was performed at 400^{o}C for 2 min using rapid thermal annealing. Annealing was found to reduce the oxide charges from $1.87x10^{-5}$ to $2.54x10^{-6}$ C/cm^{-2} and shifted the flat band voltage from – 2.67 to –0.38 V. Defect density was measured using DLTS and reported as $1.2x10^{10}$ cm^{-2}eV^{-1}. This is much lower than what is reported by other researchers (~10^{11} eV^{-1}cm^{-2} by Sung and Pang [15], $5x10^{11}$ eV^{-1}cm^{-2} by Salbert et al [10]). In an another experiment by Kunio et al, defect density measured was ~ $3x10^{10}$ eV^{-1}cm^{-2} at the mid band gap of silicon.

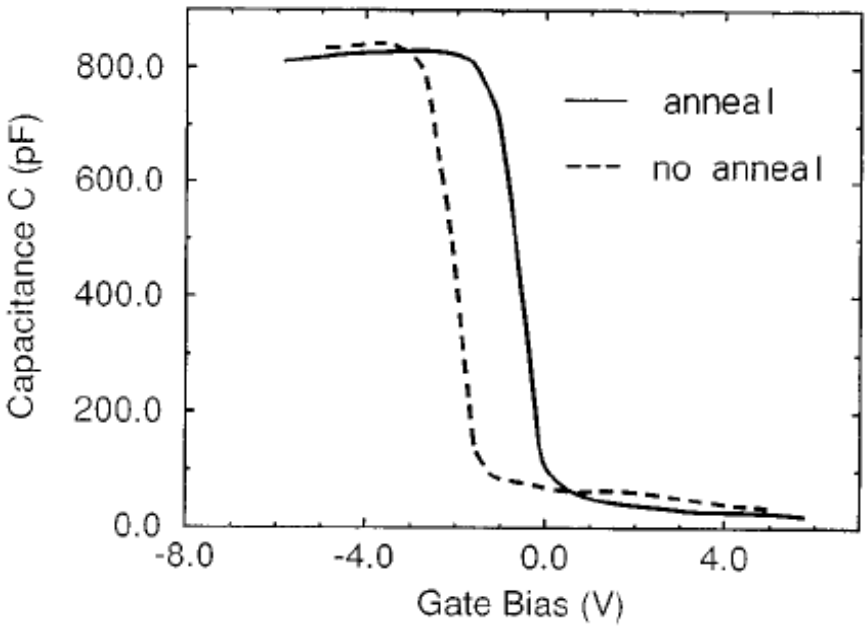


Figure 2.3 2: MOS *C–V* characteristics at 1 MHz [12].

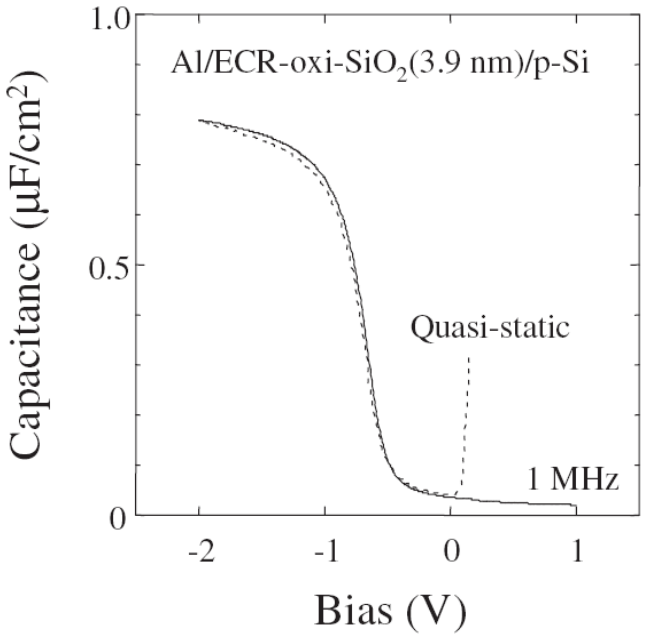


Figure 2.3 3: MOS interface defect density measurement using Quasi *C–V* and high frequency C-V curves [22]

2.4 GROWTH MECHANISM

In past thermal oxidation of single crystalline Si has been studied extensively by many researchers [55]. In particular, growth mechanism and growth kinetics [44, 45, 46], and oxide interface with Silicon wafer [40] was examined in details. Growth models have been predicted for both thin [60] and thick oxide layer [36]. Following the theories developed for the thermal oxidation, a parallel theories were tried to explain during plasma Anodization of silicon [21, 29, 30]. However, for several plasma oxidation processes, due to inherent nature of plasma generation for different plasma, growth mechanisms also turn out to be different.

In this section, we have review some of the key results from past to understand the growth mechanism of the ECR plasma oxidation of Silicon. Widely adopted model form Deal-Grove for thermal oxidation, does not fit well with the growth results observed during the ECR plasma oxidation. Kimura et al [8], [9] explained the ECR plasma oxidation growth results using Mott-Cabrera model [38]. This model assumes the movement of metal ions responsible for the thin metal oxidation layer. Using the same principle, the drift of O^- ions through the oxide layer because of the self bias generated across the oxide layer was conceived as the oxide growth mechanism.

Carl et al also studied the kinetics and mechanism of oxide growth by studying the effect of bias on ECR plasma oxide growth [13]. Oxides were grown on single crystal Si wafers at temperatures ranging from 250 to 400^oC using 2.45 GHz, 800 W microwave power supply. Source to holder distance was 14 cm. The holder was covered by a 3.2 mm thick Quartz plate with a 50 mm opening 7 mm away from the wafer surface, such that only the wafer faces the discharge, so current and voltage are only applied to wafer.

Oxides were grown for anodic, floating and cathodic condition. It was determined that only anodic and floating condition gave device quality oxide. Higher growth rates were obtained for positive dc biases. Growth kinetics was found to be limited by O^- ion movement through the oxide layer.

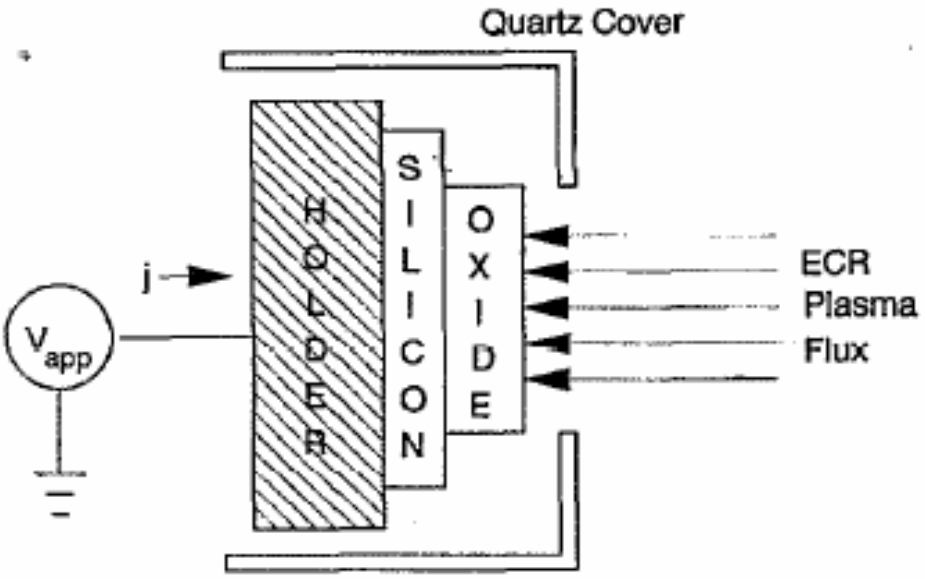


Figure 2.4 1: Schematic diagram of biasing system used [13]

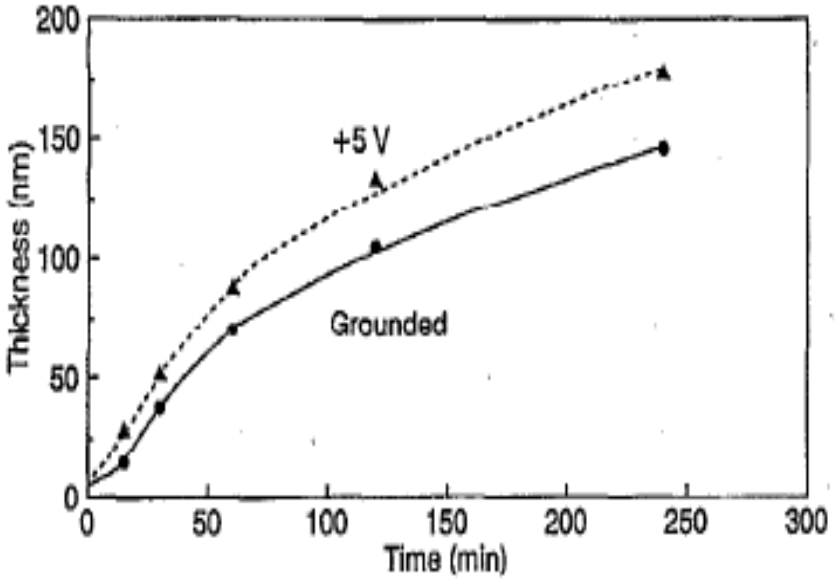


Figure 2.4 2: Effect of dc bias on oxide growth [13]

2.5 EFFECT OF FLUORINE ON OXIDATION

Kouvatsos et al. studied the influence of fluorine on thermal oxidation of Si [24]. They used the oxygen and NF_3 gaseous mixture in a temperature range of 800-1000^oC to see the effect of NF_3 gas on the growth kinetics and on the film stress. Figure 2.5.1 shows that the oxidation rates were enhanced, compared to the dry oxidation process, due to the addition of small amount of NF_3 gas. Figure 2.5.2 shows the reduction in stresses by adding fluorine.

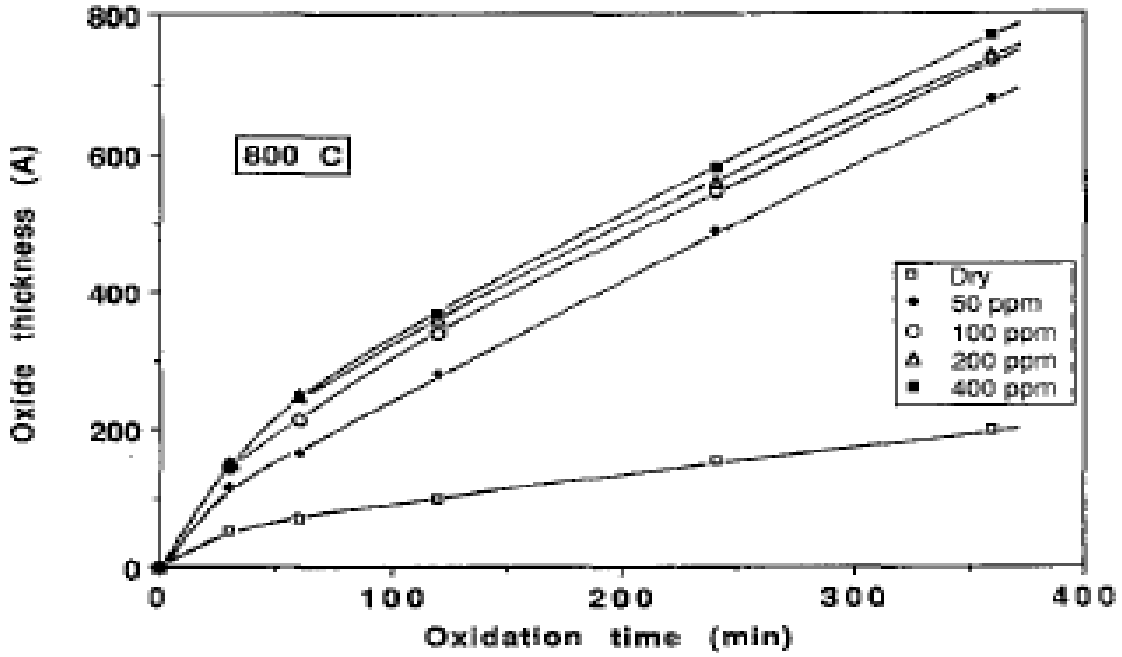


Figure 2.5 1: Presence of fluorine during thermal oxidation increased the growth rate [25]

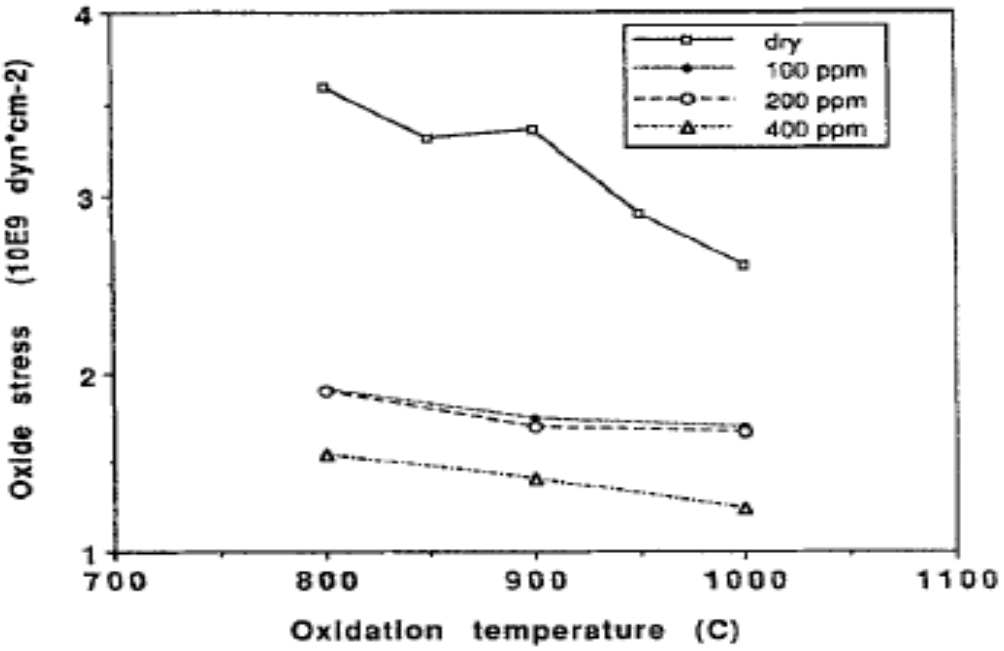


Figure 2.5 2: Stresses present in the oxide films reduce when fluorine was present during oxidation [24]

Chang et al. studied the effect of CF_4 gas on the plasma oxidation of Si [23]. The Bell laboratories linear plasma device was used for Si oxidation. Oxygen plasma was formed at a back ground pressure of 2 mT. The schematic of the reactor used is shown in Figure 2.5.3. A 300 W power at RF frequency of 20-30 MHz was applied between the Al metal electrodes. Plasma was confined by external magnetic field of 500 G. The plasma column was 5 cm in diameter and 50 cm long.

It was found that for most part (up to ~1600Å) the growth was in linear region. From this result it was inferred that growth was reaction rate controlled. The growth was also observed to be a very strong function of temperature and electric field across the oxide [23]. Oxide was not tested for any electrical measurement. See Figure 2.5.4 on next page for growth result as a function of CF_4 concentration in plasma.

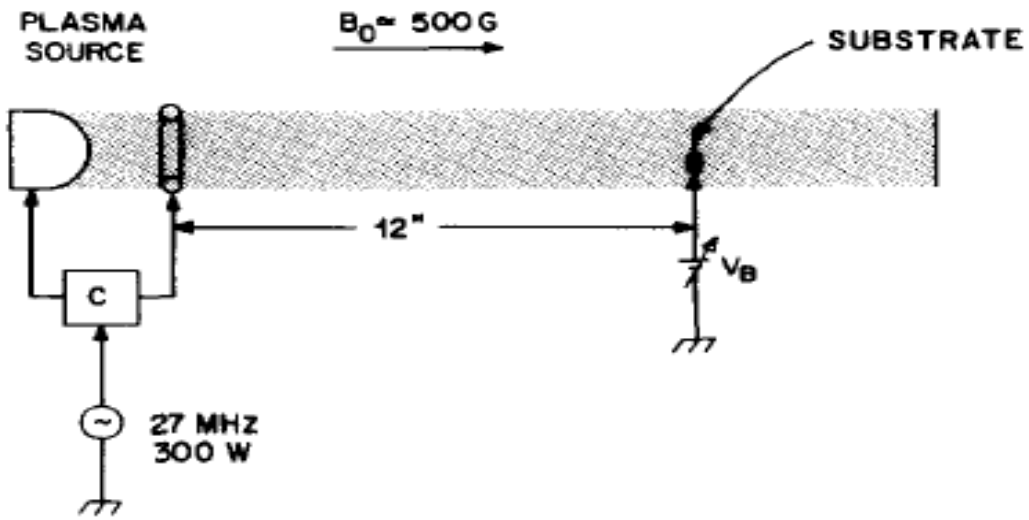


Figure 2.5 3: Schematic of the plasma reactor used [23]

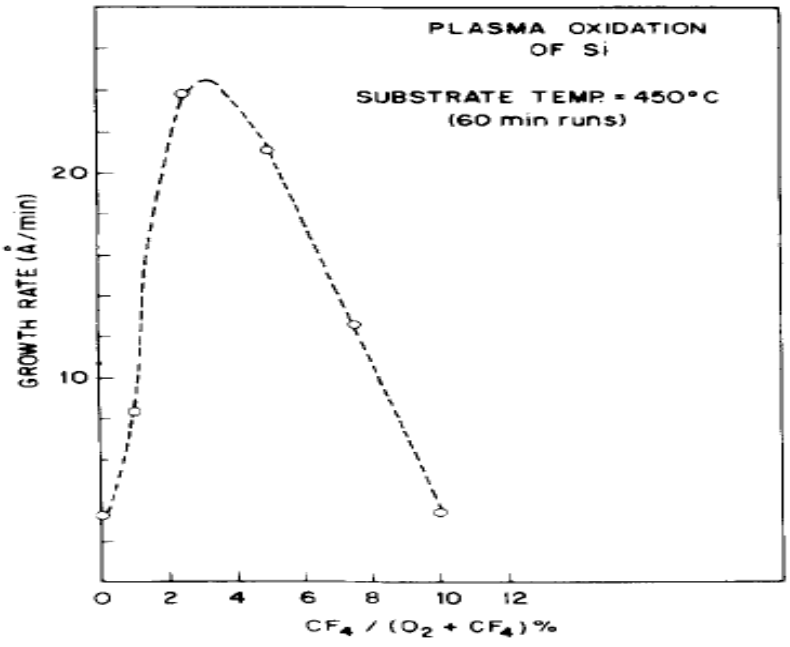


Figure 2.5 4: Increase in growth rate during plasma oxidation of Si in the presence of CF_4 gas [23]

Dalal et al. oxidized the Si using plasma of oxygen/helium gaseous mixture in presence of fluorine gas. They studied the effect of fluorine gas on Si-SiO_2 interface [27]. They used ECR plasma reactor [27] with 125 W of microwave power at the pressure range of 1-5 mT. MOS capacitor devices were fabricated and measure for the interface defect density. It was reported that the ECR oxide with fluorine gas has much lower defect density when compared to the ECR oxide with no fluorine.

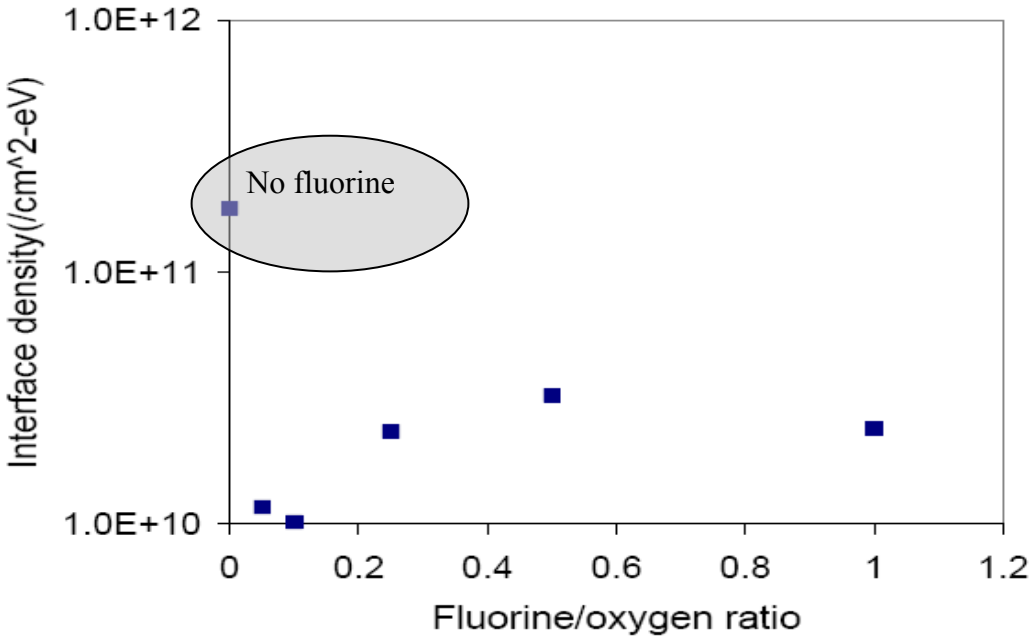


Figure 2.5.5: Fluorine during the ECR plasma oxidation was found to reduce the defect density [27]

CHAPTER 3. ECR PLASMA REACTOR

Plasma assisted processes have been extensively used in semiconductor industry to perform various operations including thin film deposition, etching and cleaning etc. High throughput and sub-micron size features in ULSI process require higher reaction rates, higher selectivity and lower damage to the substrate. In order to meet these demands, one needs plasma source of less energetic ions with high ions density. In traditional DC or capacitively-coupled rf plasma sources ions energy increases as the ions density is increased. In order to meet such demands, high density plasmas (HDP), in which ions flux can be independently controlled from the ions energy, have been developed. HDP plasmas operate at low pressure (1-10mT) which helps in achieving high plasma density and ionization rates (see Figure 3.1).

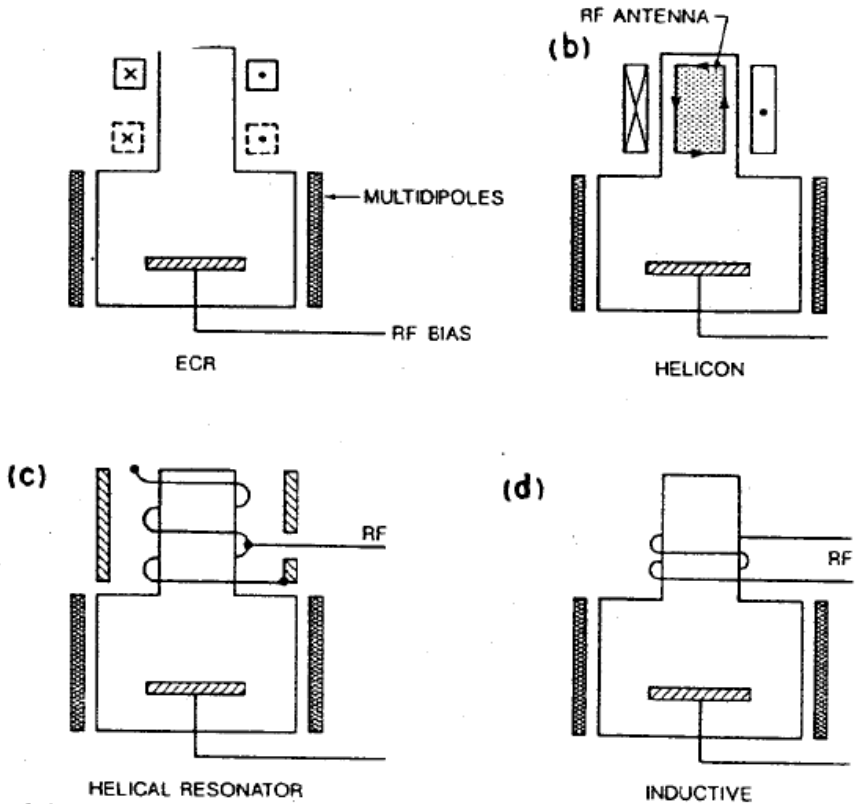


Figure 3.1: High Density Plasma Sources [67]

In HDP plasma, microwave energy is passed through a dielectric window from an external coil instead from directly from an electrode in the plasma, hence named electrodeless or remote excitation. ECR plasma used during this study is one of the HDP plasma where microwave energy coupled to a natural resonant frequency of electrons in the presence of the DC static (dc) magnetic field. ECR plasma has been extensively used in semiconductor processes such as deep reactive ion etching (DRIE), photoresist removal and thin film deposition.

In this chapter, ECR plasma generation mechanism and design of the plasma reactor used during this study have been discussed. Later, techniques of characterizing plasma and results from ECR plasma of oxygen obtained using these techniques have been presented.

3.1 FUNDAMENTAL OF ECR PLASMA GENERATION

In ECR plasma reactor electron are present in a magnetized microwave field under the presence of a DC static magnetic field. Microwaves are supplied through a quartz window while magnetic field is generated by the current carrying coils, circled on a cylindrical tube. To understand this coupling a brief review of electron motion under the electric and magnetic field is presented below. Suppose an electron is moving in a vacuum with a velocity component v, which is perpendicular to a uniform magnetic field, B. The electron will experience a Lorentz force in a direction, which is perpendicular to both v and the magnetic field. This will make electron to go in a circular path with a radius R_c (Larmor radius).

$$F = q.(v \times B) = mv^2 / Rc \quad \text{.....3.1.1}$$

$$Rc = m_e v / qB \quad \text{.....3.1.2}$$

Angular frequency of this motion can be calculated using the following relationship

$$\omega_o = qB / m_e \quad \text{.....3.1.2}$$

Note that Rc will increase as velocity is increased but angular velocity is independent of velocity. If the initial velocity of an electron has velocity component parallel to the magnetic field, the motion of an electron will be helical (Figure 3.1.1 b)

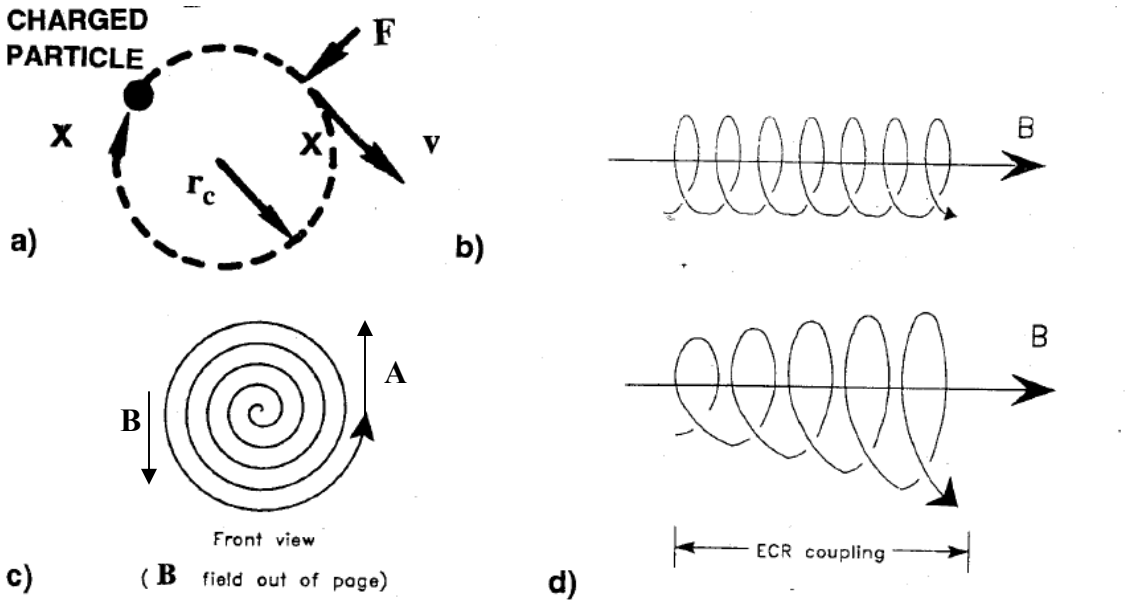


Figure 3.1.1: (a) Charge particle gyration in uniform magnetic field, **B** (directed out of the page). **(b)** Motion when the particle has an initial velocity component parallel to the magnetic field. **(c)** Increasing-radius spiral motion of a charged particle of case (a) when an E-field is applied in phase with the particle motion. **(d)** Increasing radius corkscrew motion of a charged particle having a velocity component parallel to the direction of the magnetic field, with an applied in-phase E-field.

From Figure 3.1.1, if an alternating electric field, in parallel direction to electron velocity, is applied on electron when it is a point A, it will accelerate it and velocity will be increased. Let assume that the electric field applied has the same frequency ω_o as that of an electron. In

that case, when electron reaches at point B, electric field would also change its direction, and would again be in the direction of the motion of the electron. This would further increase electron velocity. Remember that the angular velocity of the electron is not changing with the increase in velocity. Net result of this would be an electron moving with an increasing radius in a helical motion. The electron will gain more energy as it moves is a spiral motion, shown in Figure 3.1.1. Thus high energetic electrons can be produced in a low pressure gaseous mixture as electron will (larger free mean path) travel more distance before losing it energy by an inelastic collision. This is the basic mechanism of producing the high density ECR plasma at low pressures. The electron with frequency not same as that of an electric field would soon be lost and would not contribute to the plasma generation.

The ECR effect operates at low pressures 0.1 mT- 10 mT. At higher pressure there are way too many collisions to couple electron well the applied microwave signal. As the pressure is reduced the magnitude of electric field required to cause gas breakdown is reduced. This reduces the maximum sheath voltage of plasma created by an ECR plasma source. Using the equation 3.1.2 the magnetic field required for commercially available microwave frequency 2.45 GHz would be is 875 G.

3.2 REACTOR DESIGN

Figure 3.2.1 shows a diagram of the ECR reactor. A 300 W microwave generator operating at 2.45 GHz frequency was used to deliver microwave power to the reactor chamber. To minimize the reflected power in the chamber three stub tuners were used to match the impedance between the plasma and the waveguide. A quartz window was used to couple microwaves into the reactor chamber from the waveguide. Distance from the quartz window to sample was ~25 cm.

Magnetic field was generated by flowing DC current through two coil based magnets. The magnetic field profile was measured using a DC guassmeter and is plotted in Figure 3.2.2. As the figure indicates a magnetic field strength of 875 G, required to satisfy the ECR resonance condition, was present in the reactor. Curent carrying Cu coils were getting hot during long run time and high current. Heating would harm the insulation present on Cu coils and would lead to a short circuit. To prevent heating, magnets were cooled using a water supply from a chiller with temperature maintained at 7^{o}C. Water was circulated through hollow copper tubes coiled around the chamber and magnets.

The substrate holder was made of Inconel alloy, which can withstand temperatures above 1000^{o}C. It was heated by nine high temperature cartridge heaters to provide an operating temperature range of up to 900^{o}C. Temperature was measured using a K type thermocouple and controlled using a Watlow temperature controller. The substrate holder was electrically isolated from rest of the chamber by a silica based O-ring. In order to bias the substrate a DC voltage was applied directly on to the substrate holder. To measure the reactor pressure during the oxidation process a capacitance based pressure meter was used.

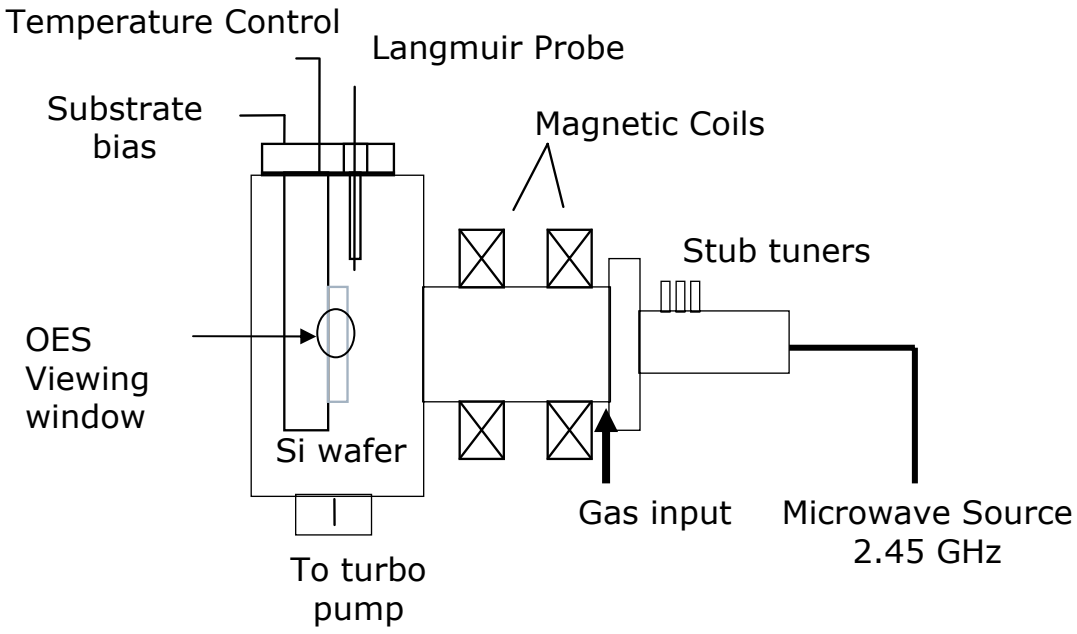


Figure 3.2.1: ECR reactor schematic diagram.

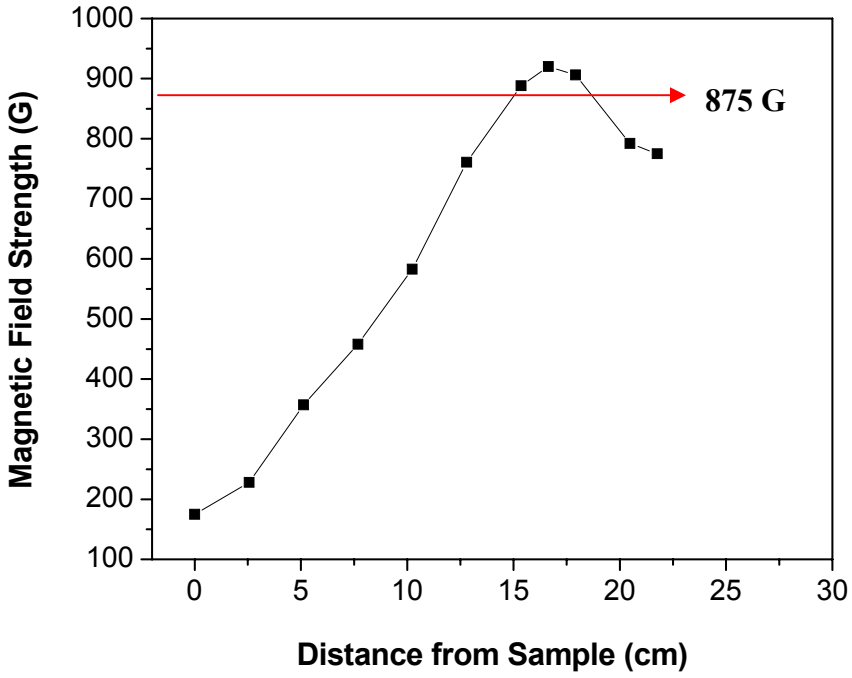


Figure 3.2.2: Magnetic field profile in the reactor.

3.3 BENEFITS OF ECR PLASMA

Listed below are some of the benefits of using ECR plasma when compared to capacitively coupled and inductively coupled plasma (ICP) sources or non-resonant plasmas.

i. ECR sources operate in 0.1 - 10 mT pressure regime as compared to 50-1000 mT for capacitively coupled and ICP plasma sources. Low pressure in the chamber reduces the number of collisions of ions in the plasma sheath and thus increases the anisotropic nature of the ions. Low pressures increase the mean free path and help electrons attain more energy before colliding inelastically with other gas molecules. Therefore these highly energetic electrons not only help in sustaining the plasma, but also provide high ionization of gases present in plasma reactor.

ii. A higher ion density $n_i \sim 10^{11}$-10^{12} cm^{-3} is achieved by ECR sources Conventional plasma sources have an ion density of $n_i \sim 10^{10}$ cm^{-3}. Higher densities mean higher ion flux driven chemical reaction rates could be achieved.

iii. We could control ion energy and ion density independently. Ion energy is controlled by applying DC or RF bias to the substrate, while ion density is varied by changing the microwave power and chamber pressure.

iv. ECR sources give lower plasma potential typically in the range of ~15-30 V. Lower plasma potential reduces the energy that ions could achieve as they traverse across the plasma sheath. Therefore damage due to ions bombarding the surface is minimized.

3.4 PLASMA CHARACTERIZATION

In any experiment it is an important step to first characterize the system in use and variation in its behavior or properties to the system inputs. In this chapter we have systematically studied the plasma parameters to better understand the process and to be able to control its properties. Before we start characterizing the plasma parameters it is a good idea to understand the basic composition of plasma. Plasma can be defined as a partially ionized gas composed of ions, electrons, and a variety of neutral species. It contains approximately equal no. of positive ions and negatively charged (negative ions and electron) species. Electron because of their low mass compared to the heavy ions, tend to have much higher kinetic energy and thus their temperature would be much higher. High energetic electron would create more plasma generation events, leading to higher plasma density, means higher concentration of reactive species available for processing.

As soon as plasma is started, electron because of their low mass gain high velocity and lost the wall of the plasma chamber. This creates a charge imbalance in the plasma and plasma becomes positively charged. These positive charges are now attracted to the negatively charged wall while electron or negative charges are repelled from the wall. This process is continued for a while and soon an equilibrium situation is achieved which creates a potential barrier for electron to migrate form plasma to the chamber wall. This self bias voltage created between the plasma and the reactor body is called as plasma potential. It can be used to access the plasma damage caused by the positive ions. Positive ions are swept by the electric field, created from this plasma potential, and hit the sample. Lower plasma potential would lead to a lesser damage to the sample.

So, reactive species composition, their density or plasma density, plasma potential and the temperature of electron are some of the important characters of any plasma system.

We characterized the Oxygen gas plasma using optical emission spectroscopy and Langmuir probe. Optical emission spectroscopy (OES) was used to identify the reactive species produced during the oxygen plasma. This enabled us to observe the variation in the plasma species densities with respect to changes in process parameters like pressure, power, and gas flow rate. Using a Langmuir probe we studied the effect of changes in process variables on plasma properties such as plasma sheath potential and plasma density. Plasma sheath potential determines the energy of ions bombarding the wafer surface and plasma density is directly related to the density of reactive species present in the plasma.

3.4.1 Optical Emission Spectroscopy

We used an optical emission spectroscopy instrument (SpectraPro-300i) from Acton Research Corporation. This spectrometer has a resolution of 0.1 nm. The plasma radiation was collected by an optical fiber. Figure 3.4.1.1 shows a typical OES plot obtained. Plasma conditions used were as follows: 1.0 mT pressure, 150 W microwave power, 5 sccm of pure O_2 gas flow rate. We found major peaks for O_2^+ at 525.5, 558.6 and 597.4 nm, and for reactive oxygen (O^*) at 394.7, 436.8, 532.9, 615.7 and 777 nm as reported earlier by Carl [11] and Kimura [8] . Carl observed the peak of maximum intensity at 777 nm with other peaks ~10 times smaller compared to it. Kimura reported a very small peak at 777 nm and rest of the peaks intensities were significantly large compared to it. In our system, we found peaks at 777 nm and others at 394.7, 436.8, 525.5, 558.6 nm of about equal intensity. The reason for such a difference is still unknown. Also in a F_2/O_2/He gaseous mixture peaks for reactive fluorine (F*) were identified at 685.6 and 703.7 nm.

We also installed a Si photovoltaic cell to measure the intensity of the plasma. This provides a quick check on plasma condition and thus helps in achieving same plasma conditions during experiments. All runs were maintained within 5% variation of this intensity.

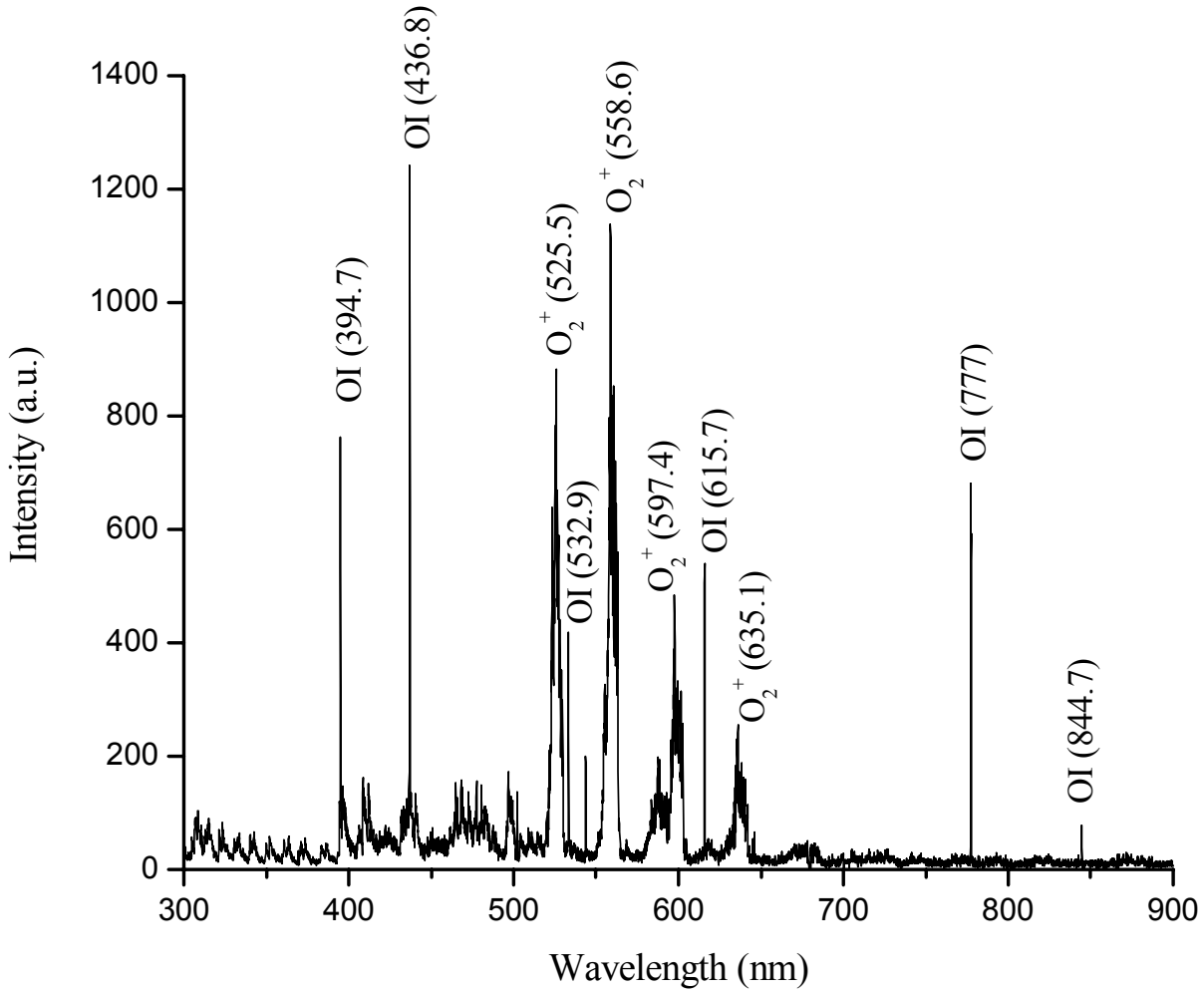


Figure 3.4.1.1: OES graph of pure oxygen plasma showing reactive oxygen and O_2^+ as reactive species present in the plasma

3.4.2 Langmuir Probe Measurement

During our experiment we measured plasma potential, electron temperature and plasma density by using a Langmuir probe. The Tantalum metal probe was 1 cm long and 0.5 mm in diameter. Current was recorded using a Keithley 2400 source-current meter as the voltage was swept from –50V to + 50V at the rate of 0.1 V/s (see Figure 3.4.2.1). We used the Laframboise method as described in [48] to calculate the plasma parameters. Based on the theory define in [48] the maximum in *dI(V)/dV* occurs at the plasma potential, $V_{maxderiv}$.

The ratio of current to the first derivative of current at plasma potential is equal to the electron temperature (eV).

$$\left.\frac{I(V)}{dI(V)/dV}\right|_{V=Vp} = \frac{kT_e}{e} \quad \text{.....3.4.2.1}$$

$$V_p = V_{\max\ deriv} \quad \text{.....3.4.2.2}$$

$$kT/e = I_{\max\ deriv} / I'_{\max} \quad \text{.....3.4.2.3}$$

To a good approximation

$$I_{0e} = I_{sat} \quad \text{.....3.4.2.4}$$

Density of plasma can be calculated using the following equation

$$I_{0e} = -en_e R_p (2\pi kT_e / m_e)^{1/2} \quad \text{.....3.4.2.5}$$

The plasma potential the as defined earlier can be determine from Figure 3.3.2. as ~6 V. Plasma density was calculated to be ~3x10^{10} cm^{-3}. Note that this density obtained near the sample is about 20 cm away from the plasma source region. Also electron temperature was in the range of 4-6 eV.

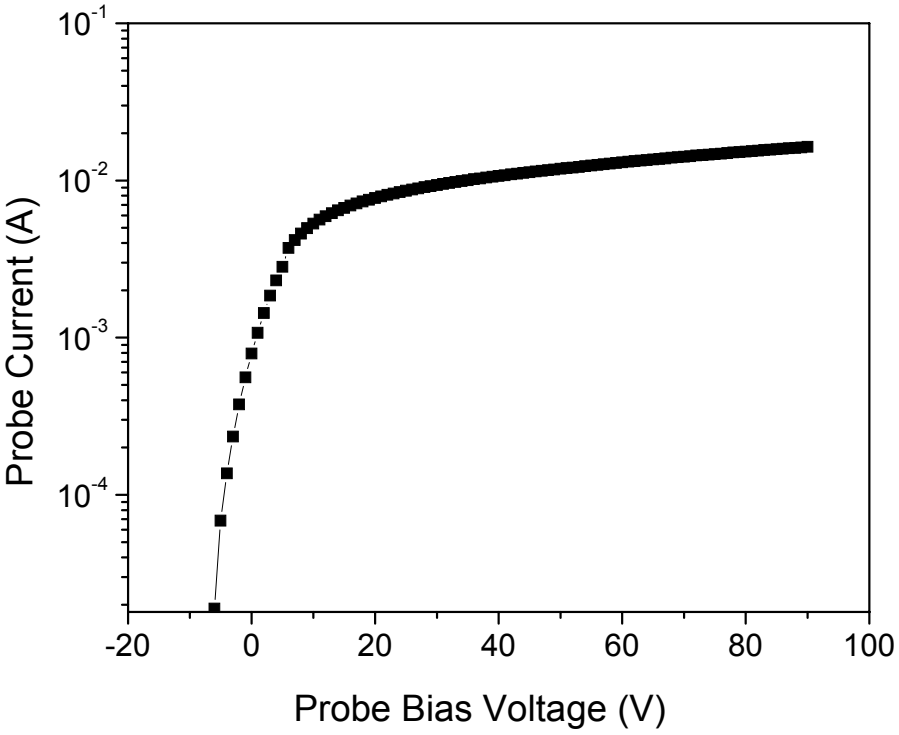


Figure 3.4.2 1: Current-Voltage characteristic of Langmuir probe used

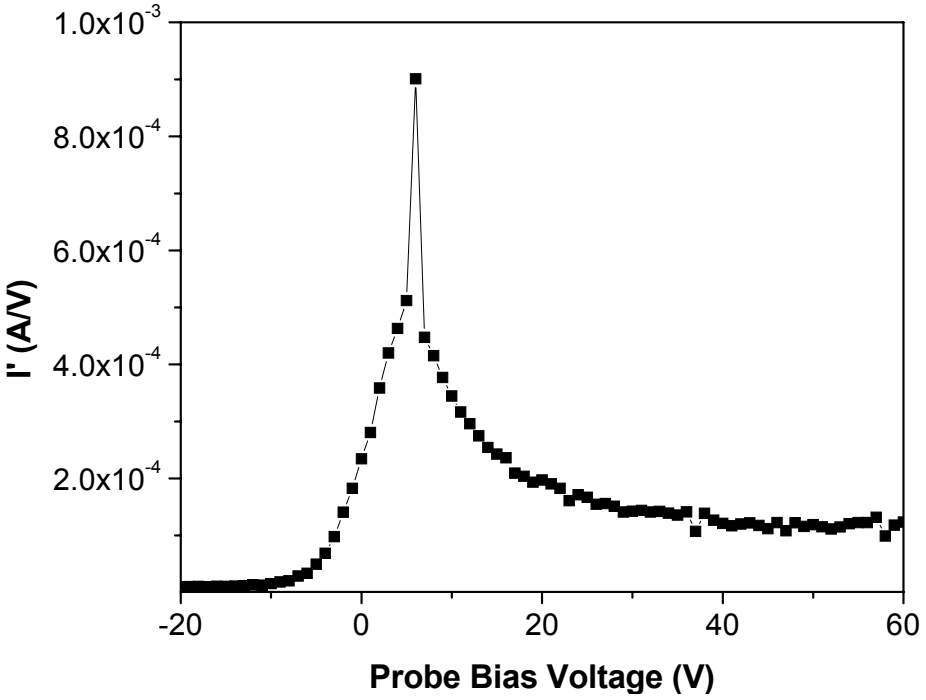


Figure 3.4.2.2: Derivative of I-V characteristic obtained using the Langmuir probe

CHAPTER 4. DEVICE FABRICATION PROCESS

NMOS and MOS capacitor devices were fabricated on a p-type Si wafer of resistivity 0.01-0.07 ohm-cm (Boron doping density $2x10^{17}$-$5x10^{17}$ cm^{-3}). NMOS devices were fabricated with dimensions (length x width) of 2 μm x 5 μm, 5 μm x 10 μm, 5 μm x 20 μm, and 5 μm x 40 μm. The dimensions of the square shaped MOS capacitor devices were 100 μm x 100 μm, 200 μm x 200 μm, and 400 μm x 400 μm. Masks were designed using L-edit and were fabricated by an outside vendor on glass. During fabrication, RCA cleaning procedures and lithography steps were performed many times. Below is the description of the RCA cleaning and lithography procedures used, followed by the fabrication process flow. For detailed instructions on the processing, refer to the MRC lab notes.

RCA Cleaning Procedure:

- SC-1: 15 minutes at 80°C: 2500 ml DI H_2O + 500 ml NH_4OH + 500 ml H_2O_2
- Cascade rinse: 5 minutes
- HF dip: 15 seconds in 50:1 HF
- Cascade rinse: 1 minute
- SC-2: 15 minutes at 80°C: 3000 ml DI H_2O + 500 ml HCl + 500 ml H_2O_2
- Cascade rinse: 3 minutes
- Spin rinse/dry

Lithography:

- Spin: HMDS at 4000 rpm for 40 seconds
- Spin: AZ 5214 photoresist at 4000 rpm for 40 seconds
- Pre-bake: 110 °C for 1 min
- Expose: 85 seconds
- Develop: MIF-312 1:1.2 developer for 60- 90 seconds
- Post-bake: 120 °C for 5-10 minutes

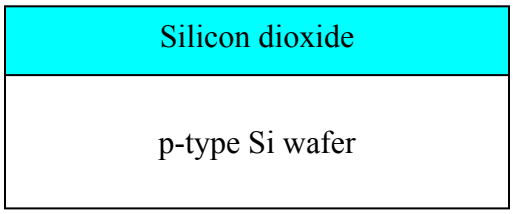
PROCESS FLOW

i. Base Oxide Formation

a. RCA cleaning

b. Wet oxidation

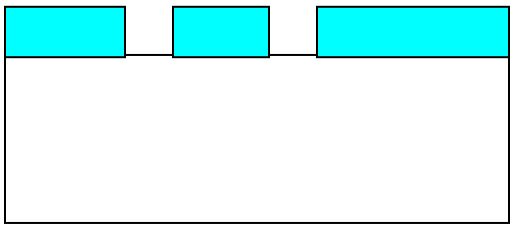
- Push- Ambient: 1 lpm N_2, Temperature: 800 °C, Time: 6 min
- Source- Ambient: 200 sccm H_2O vapor, Temperature: 1100 °C, Time: 15 min
- Pull- Ambient: 1 lpm N_2, Temperature: 800°C, Time: 6 min



ii. Pattern for NMOS Source/Drain

a. Lithography: Mask set 1

b. BOE: 10-15 minutes

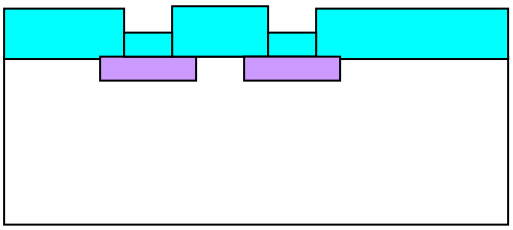


iii. N^+ (Source / Drain) Deposition:

a. RCA cleaning

b. Phosphorus Deposition

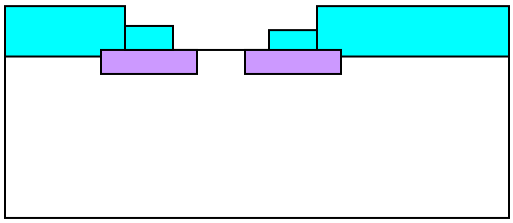
- Pull- Ambient: 1 lpm N_2, Temperature: 925°C, Time: 3 min
- Source- Ambient: 1 lpm N_2, Temperature: 925 °C, Time: 8 min
- Push- Ambient: 1 lpm N_2, Temperature: 925 °C, Time: 3 min
- Deglaze- BOE: 2 min, DI water rinse: 3 min



iv. Pattern for Gate Oxide:

a. Lithography: Mask 2

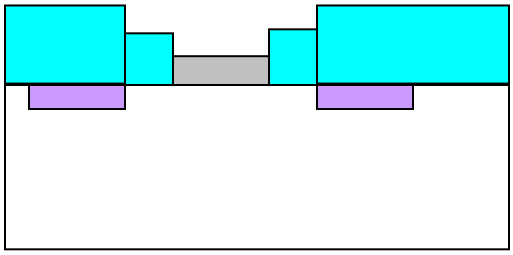
b. BOE: 10-15 minutes



v. Gate Oxide Growth:

a. RCA cleaning, HF dipped, Water rinsing

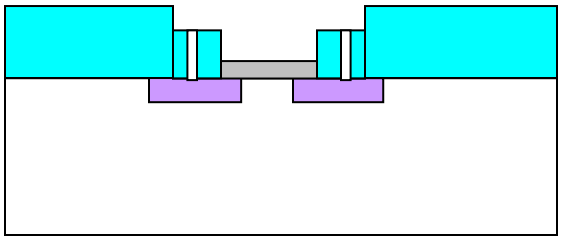
b. Oxide growth using ECR plasma



vi. Pattern for Contact Vias:

a. Lithography: Mask 2

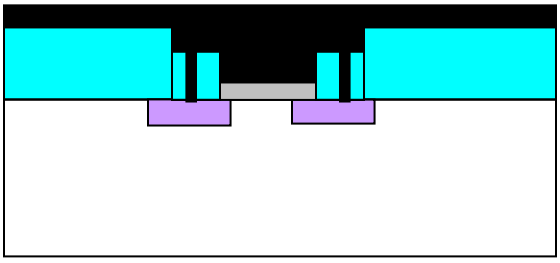
b. BOE: 10-15 minutes



vii. Contact Metallization:

a. Metal deposited: Aluminum, using thermal evaporation

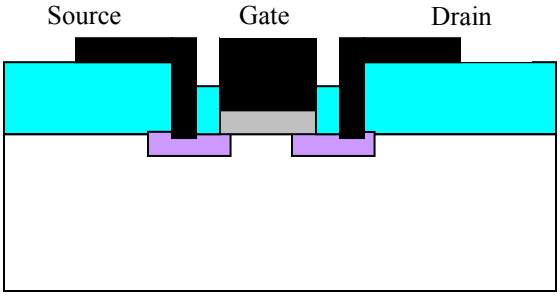
b. Total thickness: ~ 2000 Å, Pressure: 3 x10^{-6} T



viii. Pad Formation:

a. Lithography: Mask 2

b. PAN etch: 3-5 minutes



ix. Annealing: Ambient: N_2 or 3% H_2/N_2 at atmospheric pressure, Time: 30 min, Temperature: 450^{o}C.

CHAPTER 5. MEASUREMENTS

MOS and MOSFET devices were fabricated (see chapter 4) to measure the electrical properties of silicon dioxide. Physical and structural properties were studied using FTIR and XPS instruments. In this chapter, the brief description of the measurement methods used and theory behind the measurements is presented.

5.1 THICKNESS MEASUREMENT

Ellipsometer was used for thickness measurements. Because of the limited capability of the instrument available; thickness was calculated assuming the refractive index of silicon dioxide as 1.46.

5.1.1 Theory of Operation

Ellipsometer is a true contactless, noninvasive technique [39]. It is used to measure the refractive index and thickness of thin films. The principle of operation of an Ellipsometer is illustrated by the schematic drawing of the Ellipsometer shown in the Figure 5.1.1. Ellipsometer relies on the fact that the reflection at a dielectric interface depends on the polarization of the light and the transmission of light through a transparent layer changes the phase of the incoming wave depending on the refractive index of the material.

Laser beam is first passed through the polarizer, which allows only a known orientation of light passed to the sample. Some of the light will reflect immediately, and some will pass through to the far side of the material before reflecting. Light is then analyzed for the change in the polarization and the phase change [39].

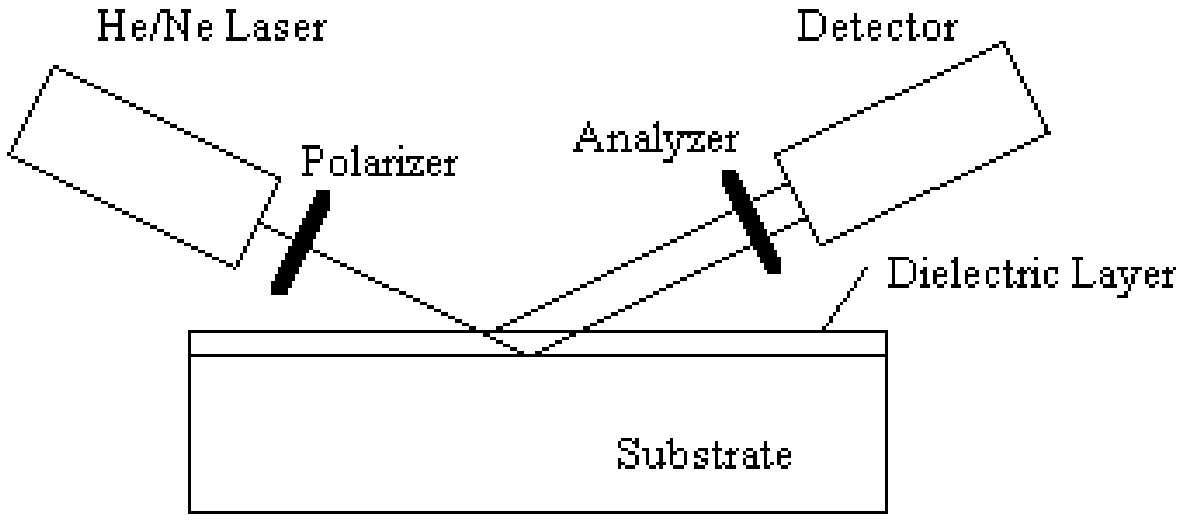


Figure 5.1.1: Basic component of an Ellipsometer

5.2 INTERFACE DEFECT DENSITY

In this section we have discussed the Si-SiO_2 structure and various charges present, methods to measure these charges and how they affect the device parameters.

Among all the MIS diodes Si-SiO_2 is by far the most important and most studied structure. But the exact nature of interface is yet unknown [41]. Figure 5.2.1 depicts a MOS interface created after the thermal oxidation of Si wafer [42]. Based on that, the chemical composition of the interface start with single crystal of Si followed by the monolayer of SiO_x, and then strained SiO_2 that is roughly 10-40 Å deep. This structure is then followed by the strain free, stoichiometric (i.e. SiO_x where x = 2 for stoichiometric silicon dioxide) amorphous silicon dioxide. These interface traps and oxide charges affect the practical MOS diode capacitance characteristic and a measure of this change could estimate the amount of these non idealities density.

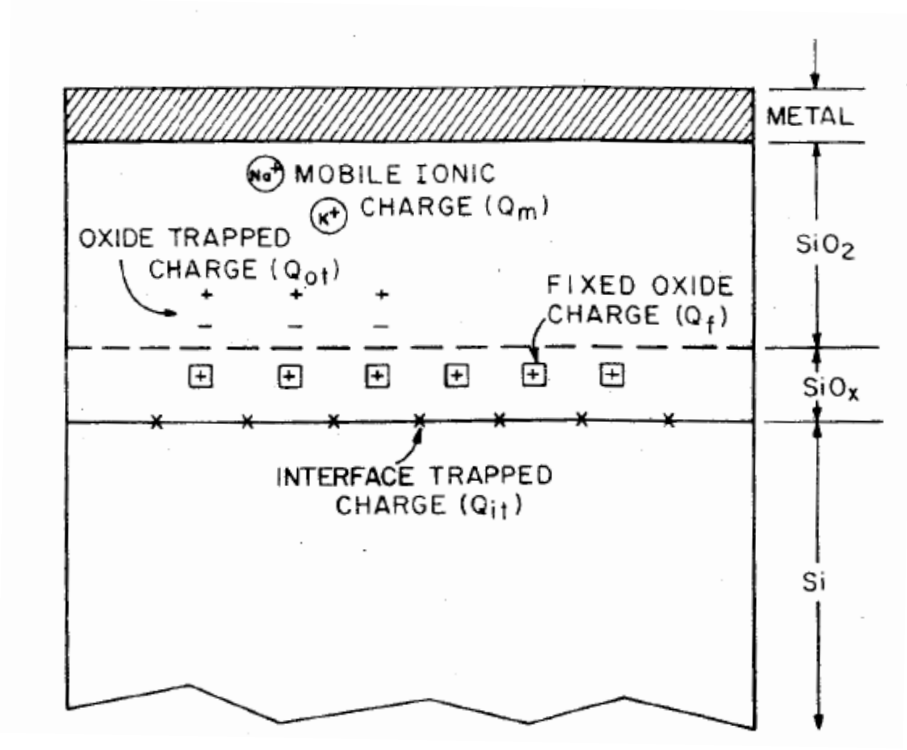


Figure 5.2.1: Types of charges present in SiO_2-Si system

There are four kinds of charges present the Si-SiO_2 interface.

i. **Fixed Oxide Charges Q_f :** These are usually positive charges, located at or near the interface (with in 30 Å) and are immobile under an applied electric field [1]. They do not respond the applied voltage at the gate and do not change with time, hence termed as fixed charges. Origin of these charges is assumed from the broken ionic Si created during the oxidation process and moved into the oxide. The values of Q_f would depend on several factors e.g. orientation of Si, oxidation temperature and post oxidation annealing. Even though these charges would change the threshold voltage, the effect of these charges in today's devices has been made minimal. Assuming these charges are at the interface, the value of Q_f can be calculated from the shift in flat band voltage [69].

$$\Delta V_{FB} = -Q_f / C_{ox} = qN_f / C_{ox} \quad \text{.....5.2.1}$$

Where ΔV_{FB} is equal to $(V_{FB})_{meas}$ - $(V_{FB})_{ideal}$, C_{ox} is the oxide capacitance (C/cm^2), and N_f is the fixed charges per unit area.

ii. **Oxide Trapped Charges Q_{ot} :** These charge, present inside the oxide, are considered as neutral until they interact with injected carriers and trap them. These charges can be created from plasma-process induced radiation, by X-ray radiation or from hot-electron injection during device operation. These charges could become positive or negative depending on the charge being trapped. Hole capture cross-section is very large possibly because of the low hole mobility in oxide and also trapped hole charges are located near the surface as opposed to the trapped electrons which are distributed through out the oxide layer. Trapped holes have more insidious effect on oxide properties than trapped electrons but fortunately the injection barriers for hole into the oxide is much larger than electron. They are important form the oxide reliability point of view as they could change the V_T to go outside the device operation regime or induce catastrophic breakdown of oxide.

iii. **Mobile Ionic Charges Q_m:** These are ions, mainly alkali ionic e.g. Na^+ and K^+, which are mostly introduced during the processing of the oxide. These charges are highly mobile at temperature as high as 200^{o}C or at high electric field. Generally during the device operation both high temperature and electric field will be present. This is detrimental to the device performance as these charges will move back and forth from Si-SiO_2 interface to the SiO_2-gate interface depending on the electric field direction, and thus alter the threshold voltage. The amount of these charges depends on the cleanliness of the oxidation process. These can be minimized by using chlorinated oxidation, regular cleaning of furnace with chlorine, and using high purity chemical and gases for cleaning and further processes. The amount of these charges can be assessed by the use of C-V technique call *Bias-Temperature-Stress*. First C-V plot is obtained for a fresh device, then positive bias ~ 1MV/cm is applied to the gate at high

temperature (~200-300^{o}C) for some time (10-30 min) and C-V graph is obtained. The change in flat band voltage obtained, from this method, would determine the amount of mobile charges present in the oxide layer.

$$\Delta V_{FB} = -Q_m / C_{ox} = qN_m / C_{ox} \quad \text{.....5.2.2}$$

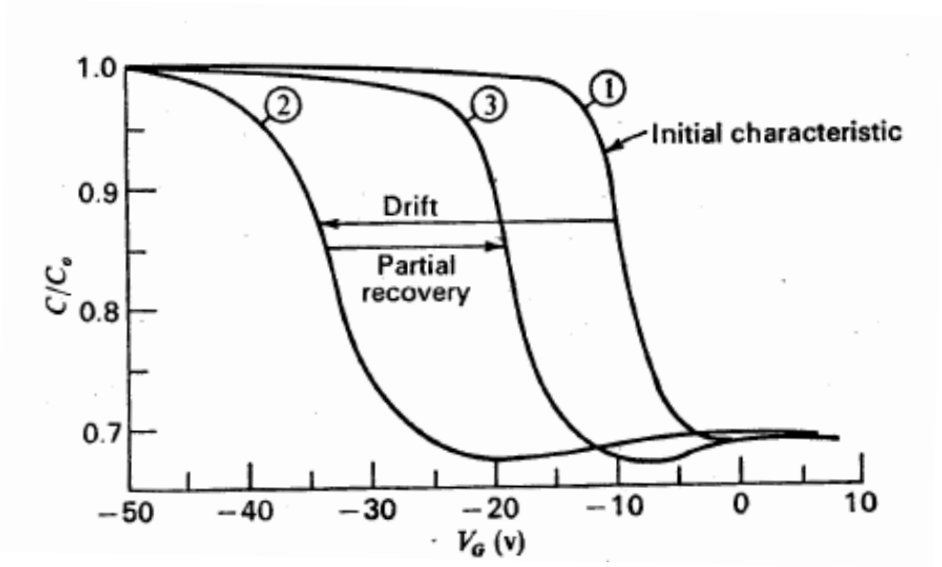


Figure 5.2.2: High frequency C-V curves showing the shift after bias-temperature stressing as a result of ionic contamination

iv. **Interface trapped charges Q_{it}**: These charges are localized to the Si-SiO_2 interface with energy states lying in forbidden band gap of Silicon. These interface state are distributed throughout the band gap of Silicon and therefore we define the term, interface trap density per unit energy, D_{it} (#/cm^2.eV). To calculate the no. of states in a given band gap we would multiply the band gap to D_{it} and that would give the no. of interface states in that band gap per unit area. Figure 5.2.3 shows the typical U-shaped defect density values from two samples as a function of band energy in forbidden band gap. As it shows, the mid-gap traps have lower defect density ~10^{10} cm^{-2}eV^{-1} compared to the trap levels near band edge which has ~10^{13} cm^{-2}eV^{-1} defect density. These interfaces traps levels above mid-gap, when

unfilled, are like acceptor. Thy become negatively charged when filled with electron and are neutral when empty. The trap levels below mid-gap are donor type and positively charged when unfilled and neutral when filled. The charge condition of the states is dependent on the Fermi level (or the applied bias). The change in threshold voltage due to these state is given by following eq:

$$\Delta V_T = -Q_{it}\Phi_{surface} / C_{ox} \quad \text{.....5.2.3}$$

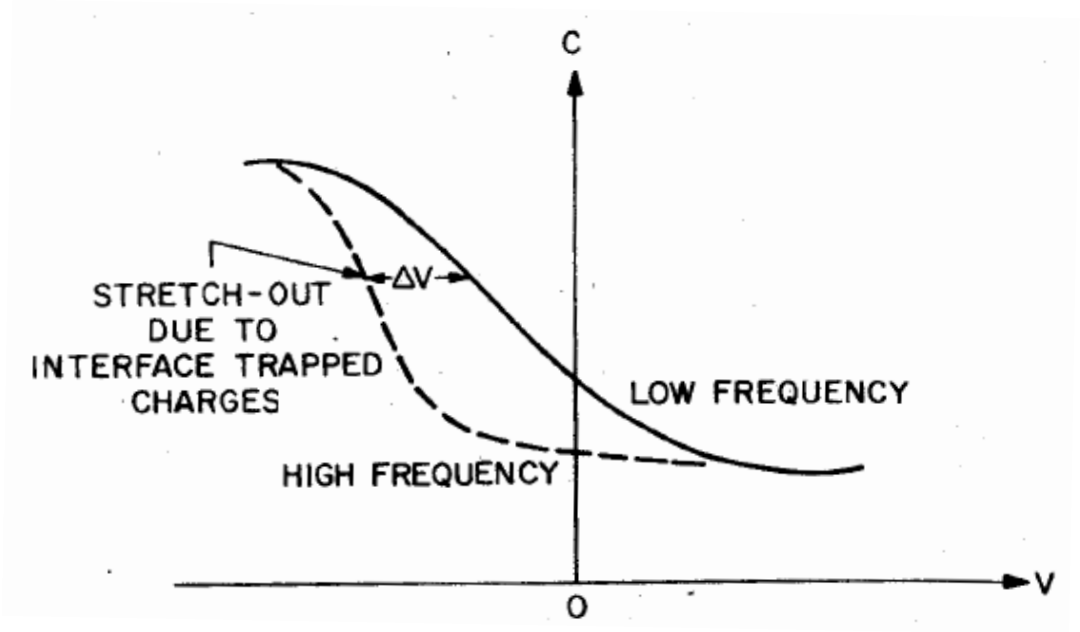


Figure 5.2.3: High frequency C-V graph showing stretch-out of capacitance region

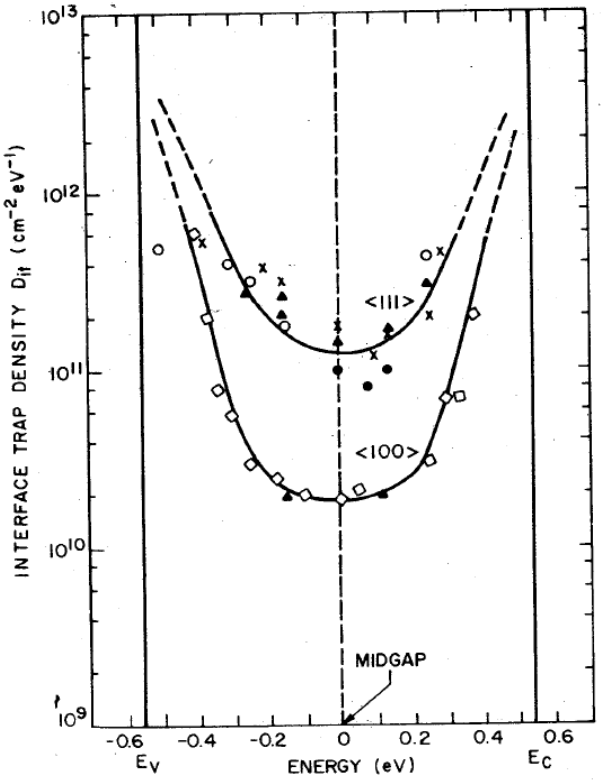


Figure 5.2.4: Typical defect density U-shaped Curve

It is difficult to measure the D_{it} from the high frequency curve alone as these charges do not produce the shift in V_T, it rather distorts the CV graph.

There generation mechanism is not well understood and it is believed that these are produced by the excess silicon (trivalent silicon), excess oxygen and impurities during the oxidation process Si atoms present at surface of Si wafer bond with O atoms to grow the oxide film (see Figure 5.2.1). During this process some of the Si atoms are not able to attach themselves with the O atoms. These Si dangling bonds act as charge trapping centers and are a major reliability concern in MOSFETs. Si <100> has ~$6.4x10^{14}$ cm^{-2} Si bonds present at the interface and if 1 out of 10,000 bonds is not attached to the O atom, number of Si dangling bonds or interface defect density would be $6.4x10^{10}$ $cm^{-2}eV^{-1}$. Si <111> orientation has higher no of bonds present at the interface and therefore has approximately 5 times

higher D_{it} levels than Si <100> orientation. Better interface with gate dielectric is one of the reasons that made the Si <100> so popular for MOSFETs fabrication.

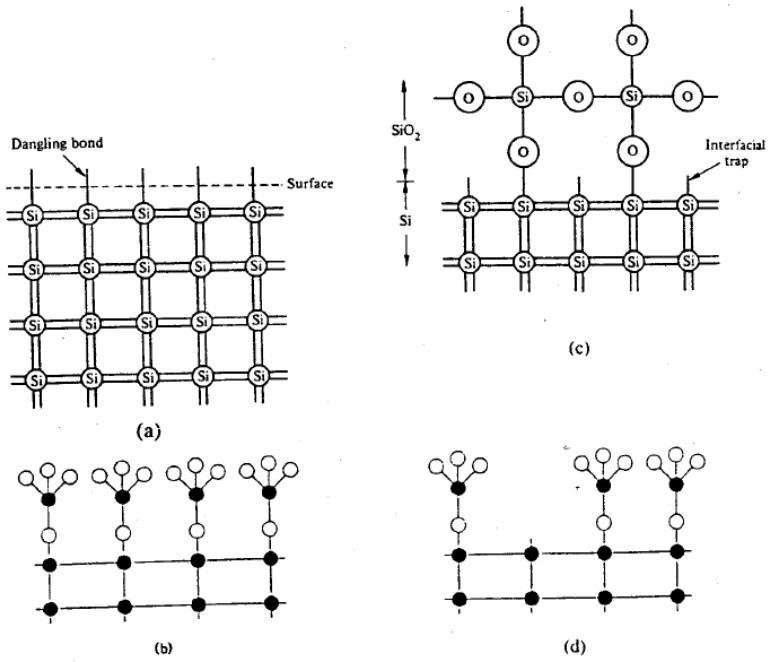


Figure 5.2.5: Figure shows the possible interface defect density generating mechanisms

The interface defect density can be brought to acceptable levels ($<10^{10}$ $cm^{-2}eV^{-1}$) by post metallization annealing (PMA) the device at ~450^{o}C tempetature in nitrogen or forming gas environment. It is believed that the hydrogen could attach to the dangling bonds at interface and reduces the defect density. But, this poses a threat to the reliability during the device operation, as week Si-H bonds are easily broken by the hot carriers.

5.2.1 Methods of Measuring Interface Defect Density

As discussed above that the interface-trapped charge exist with in the forbidden band gap due to the interruption of the periodic structure. These Qs are effective net charges per unit area (i.e. C/cm^2). To know the density one can divide this by q, and N = Q/q will be the numbers of charged per area (in cm). Because interface –trap levels are distributed across the silicon band gap, interface trap density D_{it} can be given by the following equation:

$$Dit = \frac{1}{q}\left(\frac{dQ}{dE}\right) \quad \text{.....no. of charges } cm^{-2}eV^{-1} \text{.....5.2.1.1}$$

There are several ways to estimate the interface defect density. A good discussion of all these methods has been presented in reference [34].

a. Conductance Method

b. Low Frequency Method

c. Quasistatic CV method

d. Charge Pumping Method

e. Terman Method

We used a quasistatic capacitance voltage technique to measure the defect density [45]. Capacitance-voltage graphs were obtained using a Keithley 595 Quasistatic C-V meter and a high frequency C-V graph (1MHz) was obtained using HP 4280 LCR meter. Defect density was calculated at the minimum of the Quasistatic C-V curve using following equation [41]:

$$Dit = \frac{Cox}{q}\left\langle \frac{Clf}{(Cox - Clf)} - \frac{Chf}{(Cox - Clf)} \right\rangle \text{.....5.2.1.2}$$

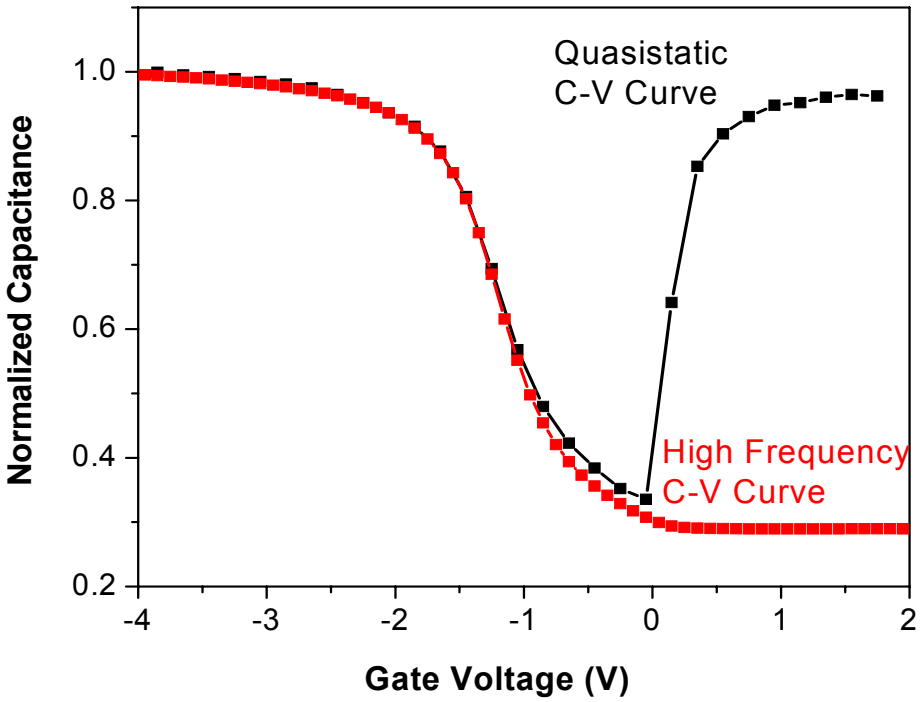


Figure 5.2.1.1: Measured quasi C-V and high frequency C-V plots

5.2.2 Theory of Operation of Quasistatic C-V Meter

The Model 595 [46] uses the feedback charge method [45] for making CV measurement. As shown in Figure 5.2.2.1, one terminal of the DUT (C_x) is connected to the voltage source and the other end is connected to the input of the feedback charge amplifier (integrator). Initially, the feedback capacitor (C_f) of the integrator is discharged by closing the switch S present in parallel with it. Switch S is opened at the starting of the measurement. Any charge transferred to the input of the integrator will now cause a change in the integrator output as follows:

$$Vout = \frac{-\Delta Q}{Cf} \qquad \text{.....5.2.2.1}$$

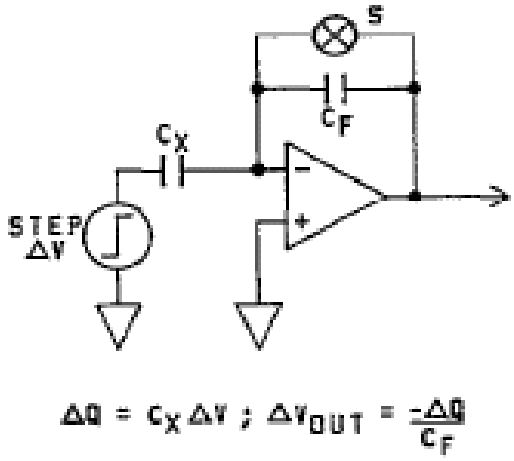


Figure 5.2.2.1: Schematic diagram of Quasi C-V measurement [46]

The voltage source is then changed by a small amount (dV) causing a charge to be transferred to $C_{ox.}$ The charge on C_{ox} is proportional to the voltage change ($dQ = C_{ox}$ x dV). The charge is then applied to the integrator and causes a voltage change at its output. The charge on the feedback capacitor is determined by measuring the integrator output voltage before and after the voltage source step and making the following calculation:

$$\Delta Q = Cf \times \Delta Vout \quad \text{……5.2.2.2}$$

C*f* is known and the unknown capacitance (Cx) is then calculated as follows:

$$Cx = \frac{\Delta Q}{\Delta V} = -\frac{Cf \times \Delta Vout}{\Delta V} \quad \text{……..5.2.2.3}$$

Because the minority carrier i.e. electron would be able to respond to the DC voltage steps, the graph would be the same as what was obtained from the low frequency curve.

5.2.3 Derivation for Defect Density Formula

Interface defects are slow and they do not respond to the high frequency. At low frequency (<50 Hz) interface defects levels are able to filled and un-filled depending on small change in voltage at any particular DC voltage. Figure 5.2.3.1 shows the equivalent circuit for a MOS device at high and low frequency applied voltage.

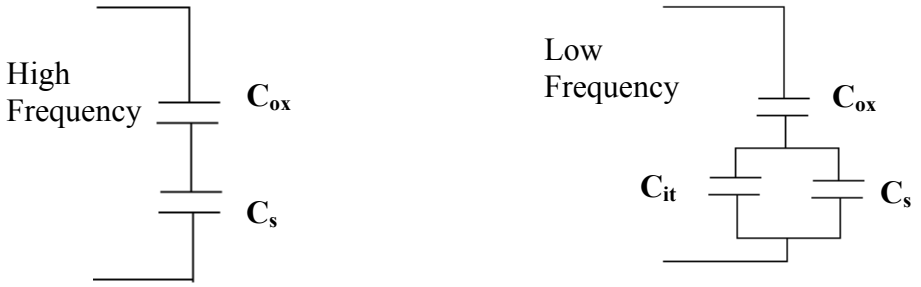


Figure 5.2.3.1: High frequency and low frequency equivalent circuit of MOS capacitor.

From Figure 5.2.3.1 one can write the equations for C*hf* and C*lf* as follows [17]:

$$Chf = \left(\frac{CsCox}{Cs + Cox} \right) \text{.....5.2.3.1}$$

$$\frac{1}{Clf} = \frac{1}{Cox} + \frac{1}{Cs + Cit} \text{.....5.2.3.2}$$

Where C_{ox}: Oxide Capacitance, C_s: Depletion Region Capacitance, C_{it}: Interface Trap Capacitance, shown in Figure 5.2.3.1

D*it* and C*s* are defined in the following equations:

$$Dit = \frac{Cit}{q} \quad \text{……..…5.2.3.3}$$

Cs is calculated from Equation 5.2.1.1 as

$$\mathrm{Cs} = \frac{\mathrm{CoxChf}}{\mathrm{Cox} - \mathrm{Chf}} \quad \text{……5.2.3.4}$$

Putting Cs from Equation 5.2.1.4 into 5.2.1.2 and using Equation 5.2.1.3 we get

$$Dit = \frac{Cox}{q}\left\langle \frac{Clf}{(Cox - Clf)} - \frac{Chf}{(Cox - Clf)} \right\rangle \mathrm{cm^{-2}eV^{-1}} \text{….5.2.3.5}$$

We can use Quasi-static graph, to get the low frequency graph, using the feedback method as described above and calculate the defect density.

5.3 MOSFET DEVICE PARAMETERS

In a MOSFET device with p-type substrate, positive gate voltage induces the electrons collection in the substrate, near Si-SiO_2 region. Threshold voltage (V_{TH}), is the minimum gate voltage (V_{GS}) required to induce this channel of electrons in the substrate. These electrons can be collected at drain end as drain current (I_{DS}), when drain is biased positive (V_{DS}). For a given V_{GS}, as the drain voltage, V_{DS} is increased I_{DS} increases linearly, assuming channel behavior to be like a fixed resistor. But at $V_{DS} = (V_{GS} - V_{TH})$, this channel breaks as threshold voltage is barely maintained near drain end, causing to drain current to saturate, I_{DSAT}. Also for a given drain voltage I_{DS} is increase as gate voltage I_{GS} is increased. Using HP parameter analyzer 4156A curves of I_{DS}-V_{DS} for constant V_{GS} and I_{DS}-V_{GS} for constant V_{DS} were collected. In this section routine to calculate the threshold voltage and linear mobility is presented.

5.3.1 Calculation of Threshold Voltage (V_T)

Threshold voltage was calculated using the I_{DS}-V_{GS} curve. In the MOSFET saturation regime $V_D = V_{Dsat} = V_{GS} - V_T$. Below is the equation for the drain current (I_{DS}) [17].

$$I_{DS} = k\left((V_{GS} - V_{TH})xV_{DS} - \tfrac{1}{2}V_{DS}^2\right) \quad \text{.....5.3.1.1}$$

$$\text{where } k = (W / L) \,.\, \mu \,.Cox \text{.....5.3.1.2}$$

V_T is voltage required at the gate terminal, for strong inversion in channel region, called threshold voltage. W and L are the width and the length respectively of the MOSFET device. Putting V_{Dsat} in Equation 5.3.1.1, drain current I_{DS} in the saturation region can be written as

$$I_{DSAT} = \tfrac{1}{2}k(V_{GS} - V_{TH})^2 \quad \text{.....5.3.1.3}$$

In Figure 5.3.1, $I_D^{1/2}$ vs. V_{GS} is plotted and value of V_T is where I_{Dsat} is zero on V_{GS} axis.

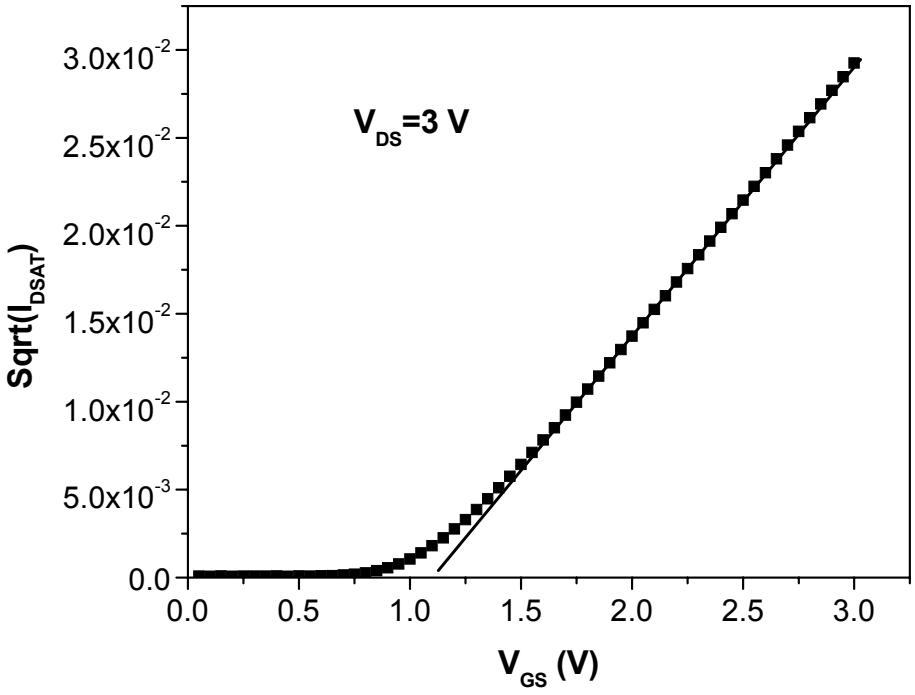


Figure 5.3.1: MOSFET I_{Dsat} vs. V_{DS} plot

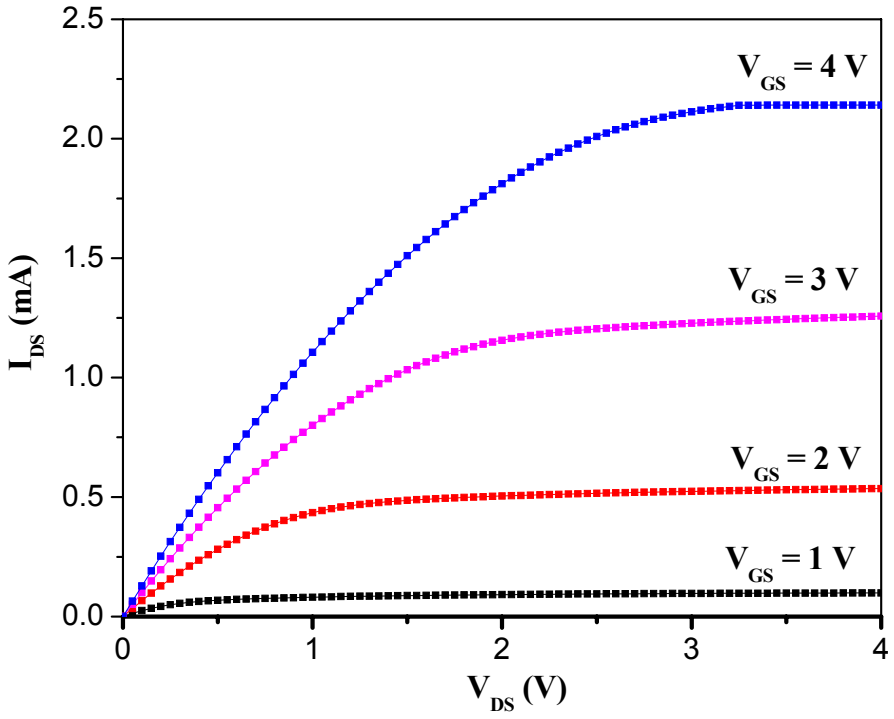


Figure 5.3.2: MOSFET I_D vs. V_{GS} plot at different V_{DS}

5.3.2 Calculations of Mobility

The velocity of electrons in a bulk Si wafer is proportional to the electron mobility under an applied electric field and the following equation can be used to calculate it:

$$v = \mu E \quad \text{.....5.3.2.1}$$

Based on above equation we need higher mobility to make faster devices. In bulk silicon electrons are free to move through out the sample and mobility can be affected because of impurities and phonon scattering. However in inversion layer electrons are confined with in a very narrow region near the Si-SiO_2 interface. Mobility of electrons in the inversion layer suffers from several other scattering mechanisms, which includes surface roughness scattering, and Coulombic scattering from the oxide and the interface charges. These additional scattering mechanisms result in reduction of the electron mobility in the channel region of a MOSFET.

In the linear region operation of MOSFET one can assume the channel to be fairly uniform from source to drain i.e. no pinch off region is present. Effective mobility is calculated from slope of I_{DS} vs. V_{DS} in the linear region (at low drain voltages, Figure 5.3.2). From Equation 5.3.1.1, at very low drain voltages we can neglect the second term in the above equation and I_{DS} can be written as

$$I_{DS} = k(V_{GS} - V_{TH})V_{DS} \quad \text{.....5.3.2.3}$$

The slope from I_{DS} vs. V_{DS} graph is equal to $k*(V_{GS} - V_T)$.

Using Equation 5.3.1.2, mobility can be calculated for given Cox and MOSFET dimensions (W/L).

5.4 OXIDE BREAKDOWN STRENGTH

One of the important properties of oxide to be used as a gate oxide is its high resistance to carrier flow [1]. It is usually of the order of ~10^{15} ohm-cm. Since it is not infinite there is always some current flowing through the oxide, which is called leakage current. For moderate gate voltages across the oxide, leakage current is very small and can be neglected. But as the oxide becomes thinner, electric fields across it increase and leakage current becomes a major problem [1].

Oxide breakdown strength is defined as the maximum electric field that oxide can withstand before breaking down. Breakdown voltage is the voltage applied across the oxide where the current density flowing through it is 1 μA/cm^2 [7]. To study the oxide breakdown strength of silicon dioxide, MOS devices of 100 μm x 100 μm area were used for this study. The experimental setup is shown in Figure 5.4.1. A constant voltage ramp (0.1 V/s) using HP parameter 4156A was applied and current is plotted in Figure 5.4.2.

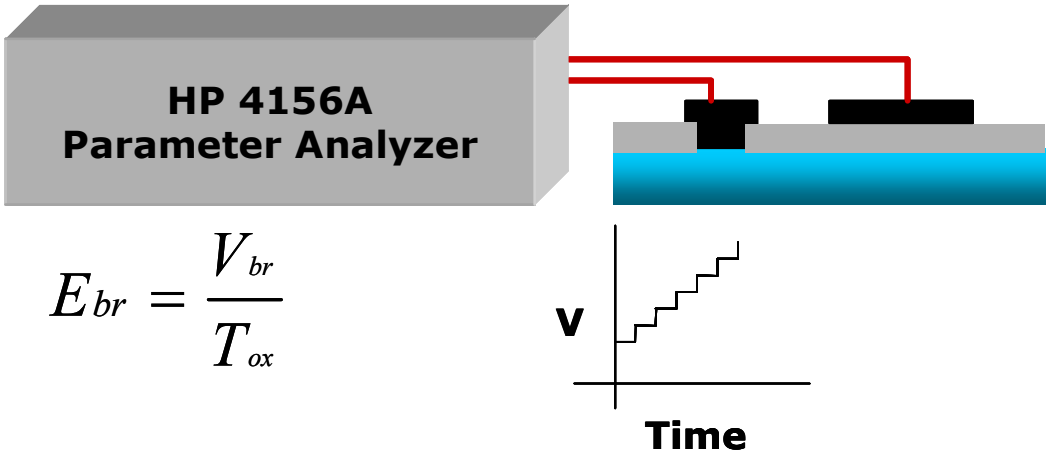


Figure 5.4.1: Experimental setup for measuring oxide breakdown strength

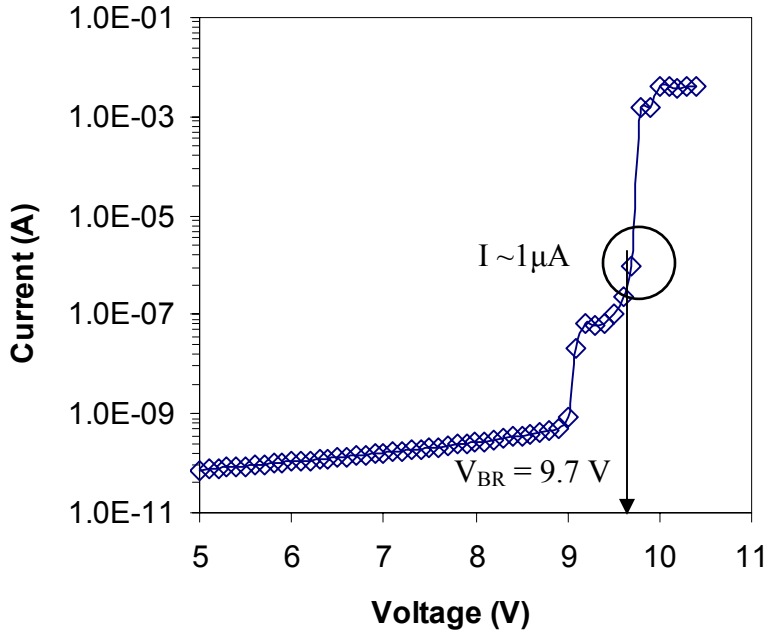


Figure 5.4.2: Current through the oxide is measured as the voltage at gate is increased from 5 V to 12 V.

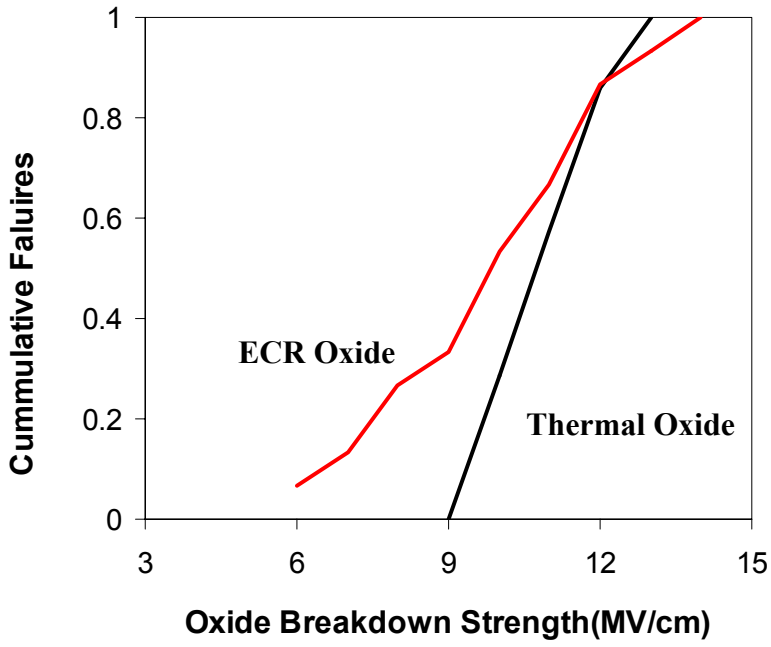


Figure 5.4.3: Cumulative Electric Field Breakdown of thermal oxide and ECR oxide

5.5 HOT ELECTRON INDUCED CHANNEL DEGRADATION

Hot channel carrier induced degradation is one of the important reliability concerns in MOSFET devices. Because of the high lateral electric field near drain, some of the electrons in the channel region obtain energies in excess of 5 eV. These high-energy electrons, called as hot electrons, can break the bonds (e.g. Si-H) present at Si-SiO_2 interface or create more e-h pairs by impact ionization in Si lattice. By breaking the bonds, they increase the interface defect densities which act as charge trapping centers. They can also be injected into the gate oxide and get trapped there. Trapping of charges at the interface and in the oxide, changes the threshold voltage and also other important device parameters. Since electrons have lower mass compared to holes they accelerate much faster and attain higher energy. The energy barrier to inject carriers into the oxide is 3.1 eV for electrons compared to 4.9 eV for holes. Thus electrons cause more severe channel degradation than holes. For this reason we have only studied hot electron induced degradation in the MOSFET channel [65].

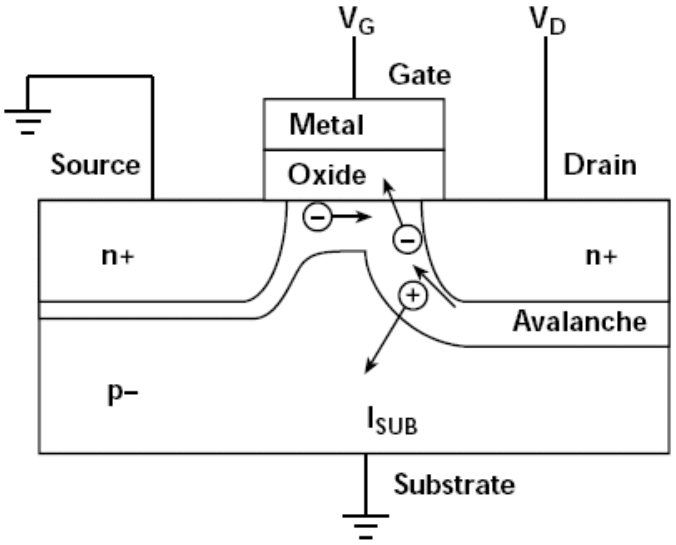


Figure 5.5.1: Degradation region near the gate/drain junction due to high electron velocity in that region [65]

Under the standard operating conditions it will take many years to see the effect of degradation on device parameters. To assess the reliability of the device we want to test it within a reasonable time period. In this section we have described how to determine the stressing conditions in order to expedite the hot electron induced channel degradation. As shown in Figure 5.5.1, holes generated from hot electron impact ionization of Si lattice are collected at the substrate end. Higher substrate current indicates that more e-h pairs are generated from hot electrons in the channel. Thus by maximizing the substrate current we can determine the stressing conditions for accelerated testing [21, 27]. Figure 5.5.2 shows a typical graph of I_{SUB} vs. V_{GS} for different drain voltages. It was determined that the substrate current was maximum at a gate voltage of $(2 + V_T)$ V for 6 V at the drain terminal.

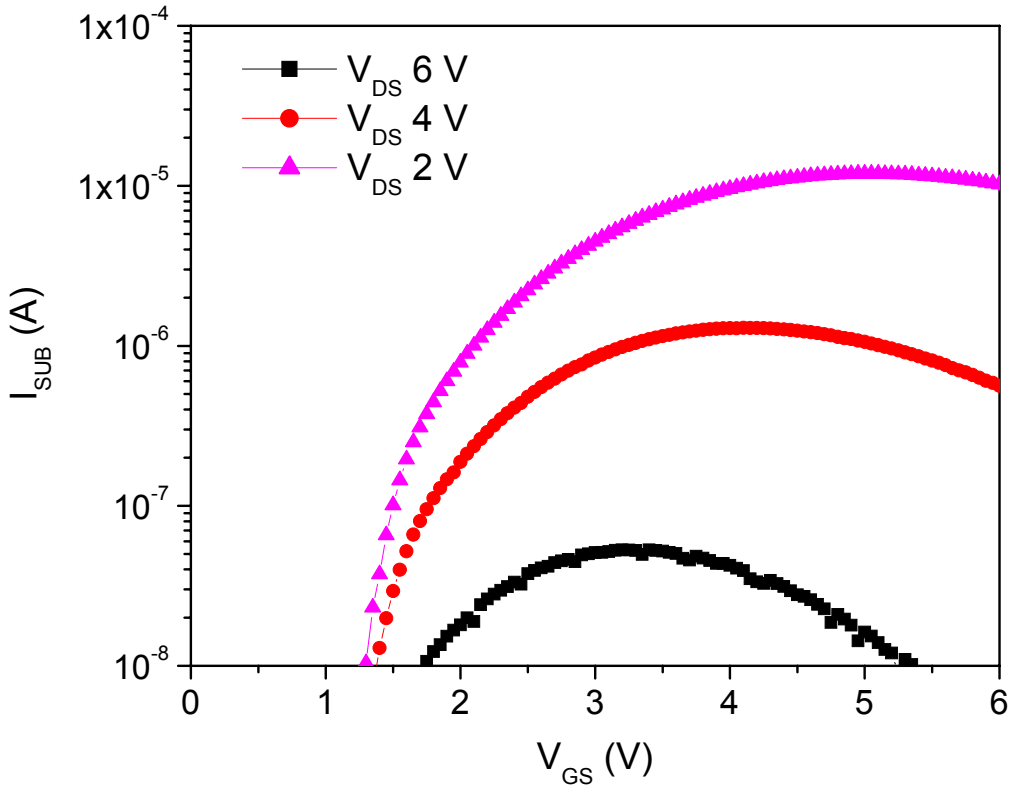


Figure 5.5.2: Substrate current measured vs. V_{GS} for different V_{DS} to determine the maximum stressing condition

Stressing was performed for up to 100,000 seconds in steps. I_{DS} vs V_{DS} and I_{DS} vs V_{GS} data was recorded at time intervals of 0, 10, 30, 100, 300, 1000, 3000, 10000, 30000 and 100000s. Threshold voltage and effective mobility were calculated using the procedure described in Section 5.3. Figure 5.5.3 shows a typical graph for change in a parameter Y with stressing time [53]. Degradation is defined as a 50 mV change in the threshold voltage or 10% change in any other properties e.g. linear mobility, sub-threshold current or effective mobility [53].

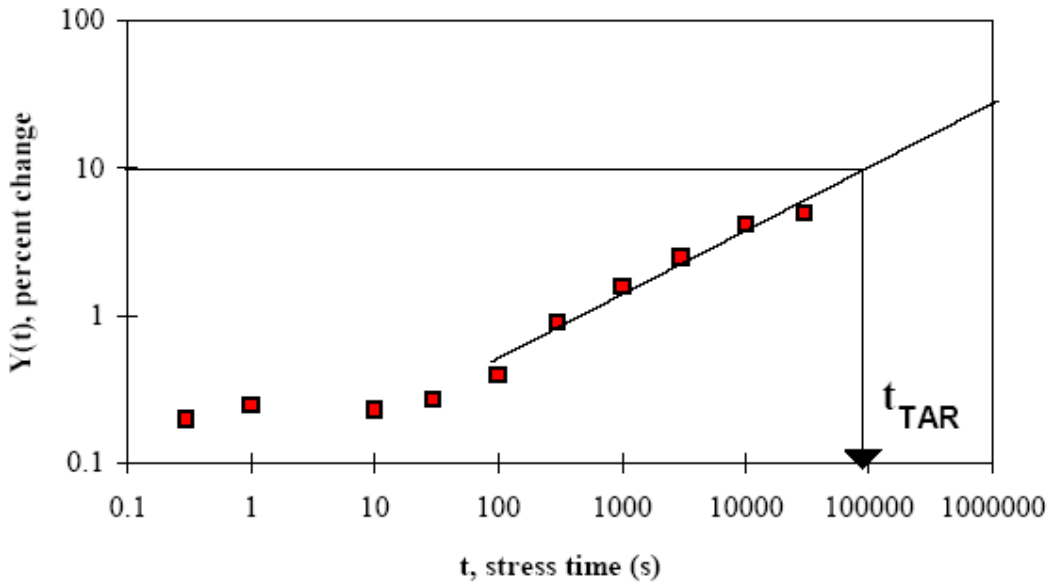
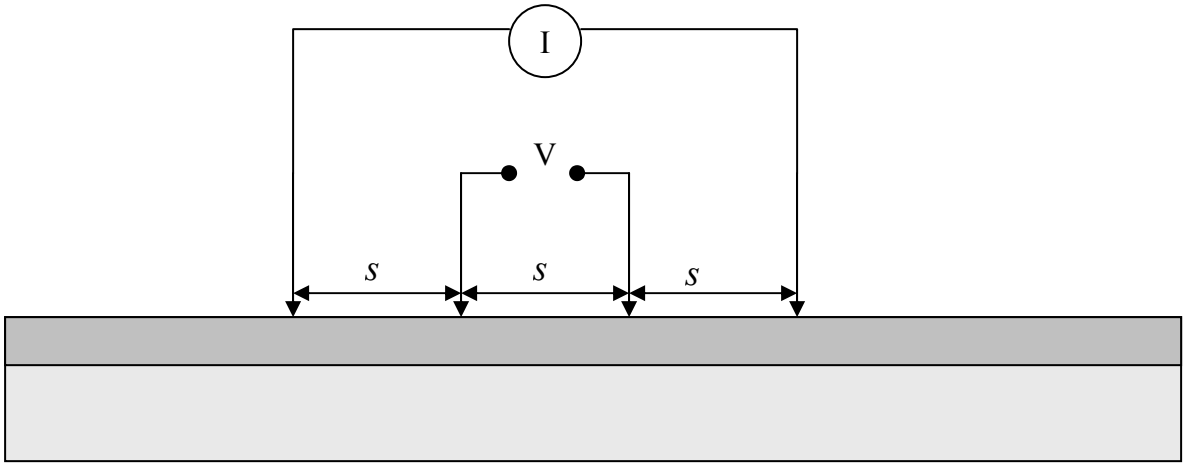


Figure 5.5.3: Typical degradation parameter change vs. time on log-log scale [53].

5.6 FOUR POINT PROBE MEASUREMNET

The four-point probe instrument is used to measure the bulk resistivity Si wafer, sheet resistance of shallow doped layer on a Si wafer or film thickness of known resistivity. It uses four probes as shown in Figure 5.6.1. Two outer probes are used to pass the current through the substrate and voltage is measured using two inner probes. This technique overcomes the error introduced when you just use 2 probes to pass current and measured voltage across them. In that case voltage drop across two probes is also from the probes resistance, contact resistance between probes and the substrate, and the spreading current resistance. While in four-point probe method, voltage is measured using a potentiometer having infinite resistance (in practice very large), thereby no current (or very small as resistance is not infinite) passes through the probes. Voltage measured is just from the current flowing through the resistive layer and hence provides only resistance of that layer.



5.6.1: Figure shows that basic setup for using the Four-point probe measurement

a. For bulk sample (s << t): resistivity given by following equation:

$$\rho = 2\pi s\left(\frac{V}{I}\right) \quad \text{.....5.6.1}$$

where V/I is the slope of the V vs. I graph.

b. For thin films (t << s):

$$\rho = \frac{\pi t}{\ln 2}\left(\frac{V}{I}\right) \quad \text{.....5.6.2}$$

where t is the thickness of the layer to be measured (t << s). For semiconductor materials, it is often presented as sheet resistance, which can be calculated as follows:

$$R_s = k\left(\frac{V}{I}\right) \quad \text{.....5.6.3}$$

5.7 X-RAY PHOTOELECTRON SPECTROSCOPY

X-ray photoelectron spectroscopy is a quantitative elemental analysis technique that uses soft X-ray to analyze the top 5-10 nm composition of the material. X-ray knocks of the electrons from the inner shells kinetic energy of the electrons emitted from the surface of the material is analyzed using an electrostatic electron energy analyzer.

Figure 5.7.1 shows the basic component of the XPS system. The X-ray, consisting of high energetic photons ~1.5 KeV, possesses enough energy to ionize the atom or the molecule it is falling on. These released electrons could come out of the surface and then collected by the electrostatic detector. The electrons, which are far deep from the top surface (~5-10 nm deep) lose their energy by colliding with near by atoms and can't come out of the material.

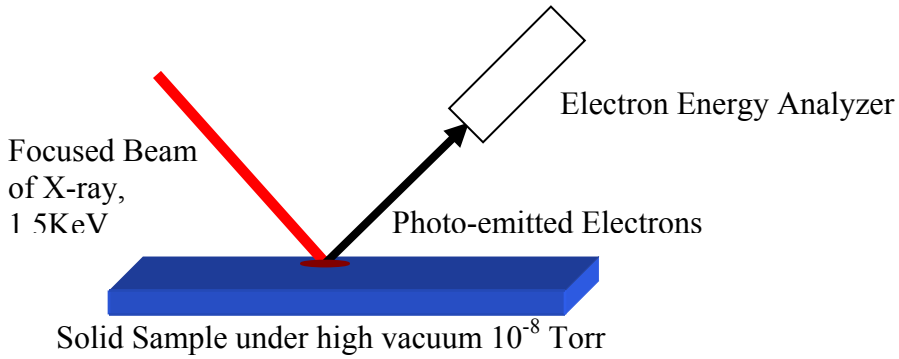


Figure 5.7.1: Basic components of the XPS system

The kinetic energy of the electron will be given by the following equation:

$$E_{\text{binding}} = E_{\text{photon}} - E_{\text{kinetic}} - \Phi \quad \text{.....5.7.1.1}$$

Where E_{photon} is the energy of the electron emitted from a particular configuration from the atom, $E_{kinetic}$ is the kinetic energy of the electron emitted; Φ is work function of the spectrometer, not the materials. Energy not the electron not only depends on the shell they are coming but also on the surrounding atoms and nature of bonding.

We used Physical Electronics 5500 Multitechnique System for XPS analysis which is available with Ames Lab. It uses monochromatic Al and standard Al sources. Energy of the Al X-ray source was ~ 1486.6 eV. Energy resolution was ~0.75 eV FWHM. Oxide layer was etched using Ar gas. On this instrument etching rate for silicon dioxide is ~10 Å/min. To get the depth profile of the oxide layer, elemental analysis was performed as the oxide film was etched.

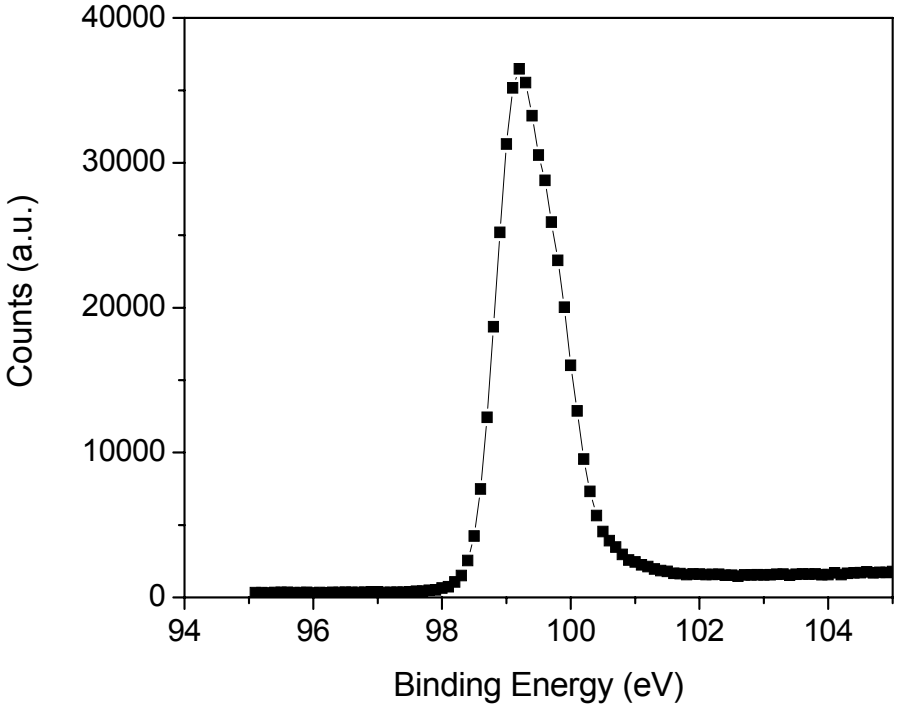


Figure 5.7.2: Binding energy of Si 2p shell electron

CHAPTER 6. RESULTS AND DISCUSSION

6.1 EFFECT OF ANNEALING ON DEFECT DENSITY

Annealing of MOS devices at high temperatures has been found to effectively reduce the interface defect density (D_{it}) and fixed oxide charges [39]. The aim of this experiment was to find the right set of annealing conditions to get the minimum D_{it}. In first set of experiments, as-grown oxide films were annealed, before gate metallization, in O_2, H_2, N_2, and $3\%H_2 + N_2$ (Forming gas) gases. Samples were annealed in 1 atm. pressure at 450^{o}C temperature for 30 minutes. MOS devices were then fabricated using Al as the gate metal. In the second set, first thermally evaporated Al metal was deposited on the oxide. MOS devices were fabricated and annealed using same annealing conditions as mentioned above. This is referred as post-metallization annealing (PMA). From the results shown in Table 6.1.2, PMA was found more effective in minimizing the D_{it} when compared to pre-PMA annealing. The reduction in interface defect density is mainly attributed to passivation of Si dandling bonds by formation of Si-H bonds at the silicon-silicon dioxide interface. During annealing in nitrogen gas, moisture present on the oxide film could lead to the ppm levels of hydrogen required for Si passivation mechanism to occur (see figure 6.1.1). Devices annealed in forming gas tend to show higher HCI degradation because of weak Si-H bonds formed at the interface during the annealing process [68]. Therefore for future runs, post-metallization annealing treatment in nitrogen gas at 450^{o}C for 30 min was set as a standard procedure.

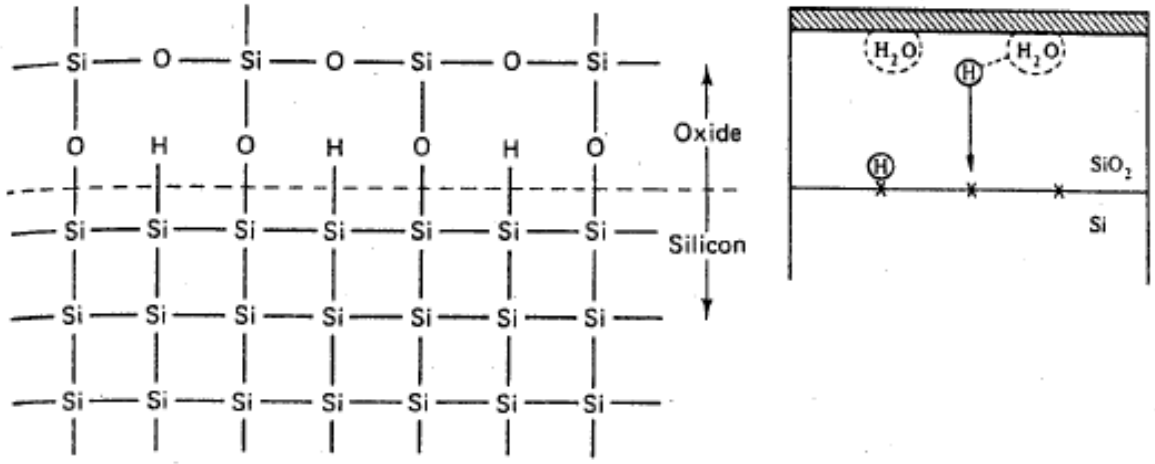


Figure 6.1.1: Hydrogen passivation mechanism of Si danling bonds at Si-SiO_2 interface [68]

Gas Used	D_{it} ($cm^{-2}ev^{-1}$) Pre-PMA	D_{it} ($cm^{-2}ev^{-1}$) PMA
O_2	1.65×10^{12}	5.88×10^{11}
H_2	5.35×10^{11}	1.81×10^{11}
N_2	1.60×10^{12}	1.0×10^{11}
3% H_2/N_2	1.19×10^{12}	8.1×10^{10}

Table: 6.1.2: Effect of pre and post metallization annealing on defect density.

6.2 EFFECT OF PROCESSING PARAMETERS ON OXIDE GROWTH

6.2.1 Effect of Pressure

Figure 6.2.1.1 shows the effect of pressure on plasma intensity and on the ratio of O_2^+ ions to reactive oxygen (O^*). Using OES technique (see section 3.4), an ~35 times increase in reactive species concentration was observed as pressure was reduced from 15 mT to 0.5 mT.

The presence of a magnetic field in ECR plasma causes electrons to travel in a corkscrew path (see Figure 3.1.1). At low pressures electrons have a long mean free path and make more loops before colliding with other molecules. This allows electrons to attain higher energies. These energetic electrons are more much more likely to produce plasma generating events (ionization/excitation) when they collide with other molecules in the plasma. This is why the intensity of the plasma, which is directly related to the density of reactive species in the plasma, was higher at low pressures.

Also the ratio of O_2^+/O^* was observed to increase at lower pressure. As explained above, at low pressures more high energy electrons are present in the plasma. Ionization process needs higher energy electron as compared to the dissociation of oxygen gas. These high energetic electrons preferably ionize the oxygen gas.

$$O_2 + e \rightarrow O_2^+ + e + e \text{……...…....(Ionization energy ~12.2 eV)}$$

$$O_2^+ + e \rightarrow O + O \text{ ……..(Dissociation energy ~ 5 eV)}$$

At the low pressure slightly thicker oxide film were formed (see Figure 6.2.1.2). However there was no one to one correlation observed for the increase in oxide thickness to the increase in plasma density. This suggests that oxidation reactions are dependent upon the transport of oxidizing species through the oxide layer or on the oxidation reaction rate at oxide-Si interface.

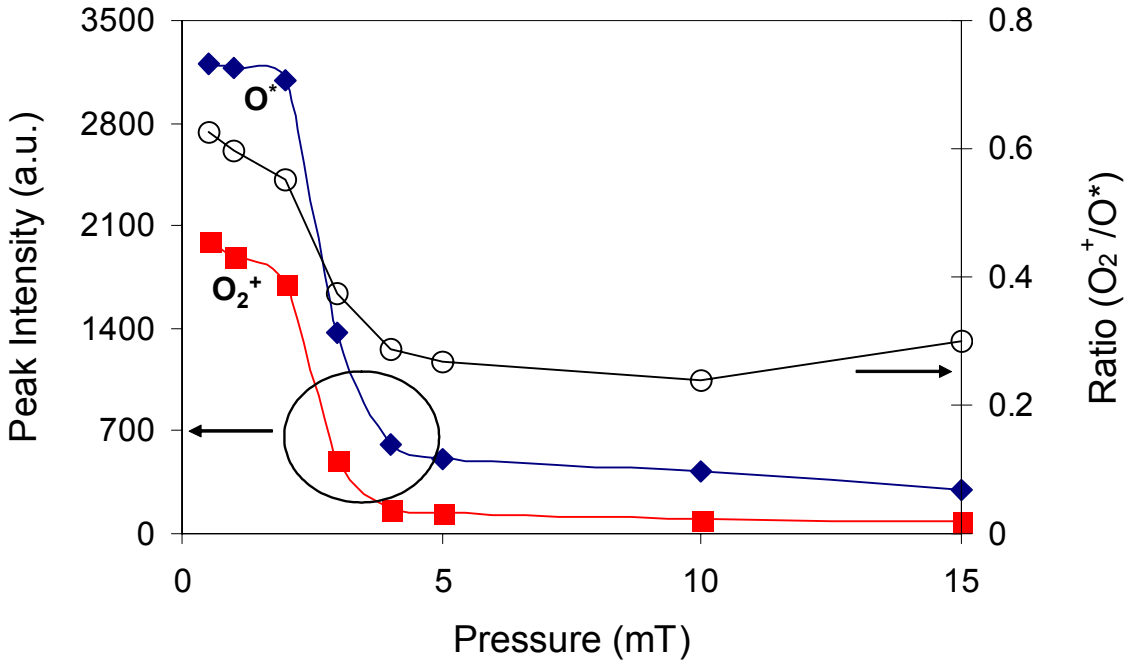


Figure 6.2.1.1: High plasma density and O_2^+/O^* ratio are obtained at lower pressure.

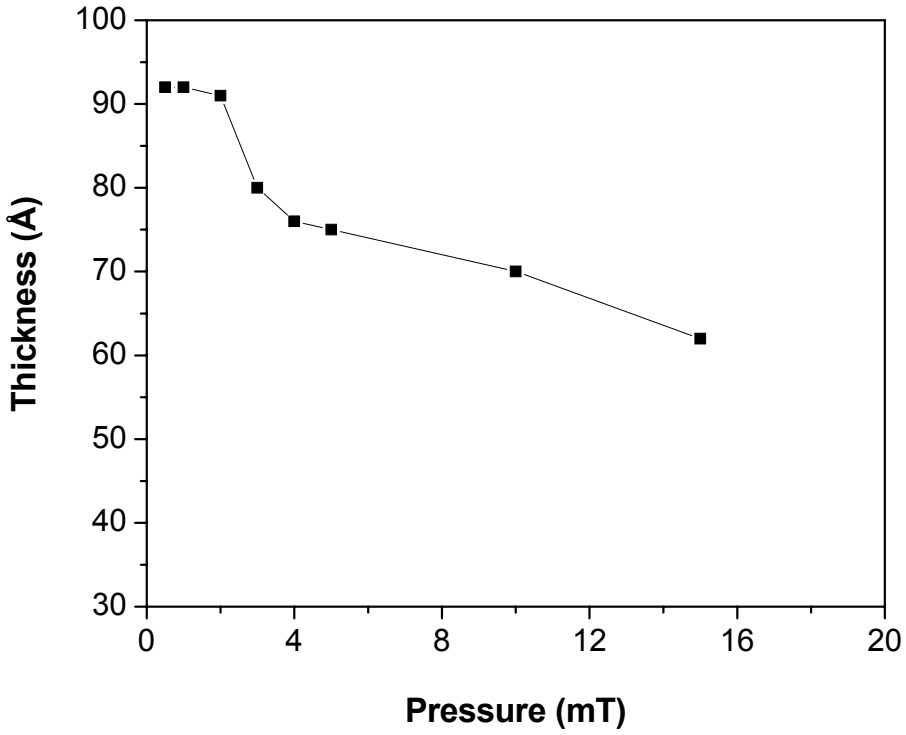


Figure 6.2.1.2: Thickness vs. chamber pressure

6.2.2 Effect of Temperature

To see the effect of temperature, plasma oxidation was performed at 100, 300, and 500^{o}C temperatures. Plasma with 150 W microwave power at 1 mT chamber pressure, and 5 sccm flow rate of pure oxygen was used. Oxide thickness was measured using an Ellipsometer as described in section 3.1. After 5 min of plasma oxidation, at all three temperatures, thicknesses were ~40 Å (see Figure 6.2.2.1). Under the measurement errors present in thickness measurements, there was no noticeable difference found in the oxide thickness grown at difference temperatures. Thus the thermal activation energy for this process is very close to zero. Similar results have been reported by Kunio [22]. For thin oxides one would expect oxidation reaction to be the rate controlling step. The low activation energy obtained indicates that even for thin oxide thickness, reactions were not thermally but plasma enhanced.

For oxide thicknesses greater than 40 Å, at low temperatures, a diffusion limited growth is expected. The activation energy for the ECR plasma grown oxide was found to be ~ 0.02 eV. Activation energy for the thermal oxidation of Si is ~1.2 eV [1]. Low value of activation energy obtained during plasma oxidation shows that the transport of oxidizing species is not thermally limited. Later, by applying DC bias at substrate holder, we establish that the transport of oxidizing species is electric field assisted. This explains the large difference in activation energies for thermal and plasma assisted oxidation processes.

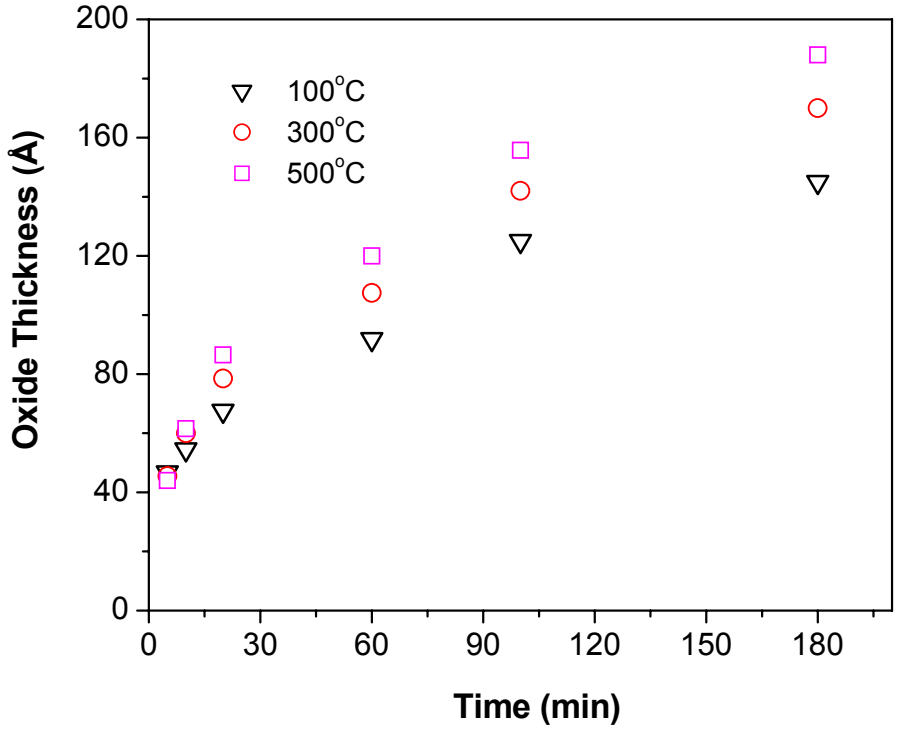


Figure 6.2.2.1 Effect of temperature on growth rate

6.3 EFFECT OF DC BIAS

Results from previous sections show that the oxidation growth was limited by the transport of oxidizing species. In this section, the effect of electric field, applied across the oxide layer, on the oxide growth is evaluated. Experiments were carried out using unheated substrate holder at 150 W of microwave power, 5 mT chamber pressures and a 5 sccm gas flow rate of pure oxygen. Special substrate holder was fabricated to ensure that only Si wafer would see the plasma (see Figure 6.3.1). There was a significant difference in the growth results obtained from the substrate holder compared to the regular stainless steel body substrate holder (see figure 3.2.1).

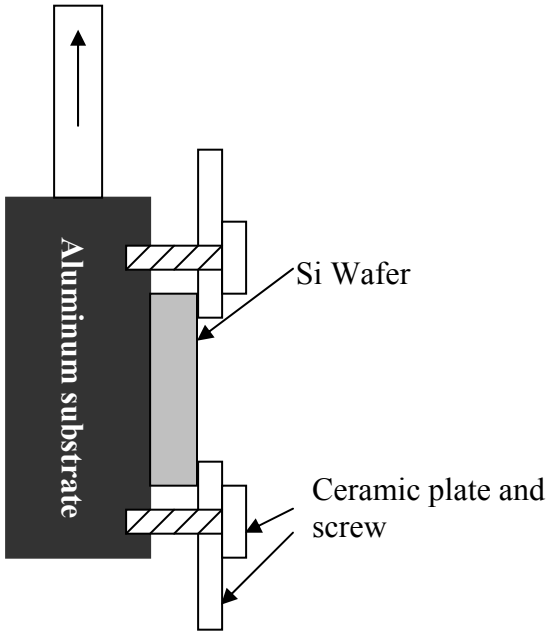


Figure 6.3.1: Schematic diagram of the new substrate holder

At –50 V DC bias on the substrate, the oxide thickness was ~32 Å after 5 min of oxidation. Oxide could grow only to 47 Å even after 180 min of oxidation (see Figure 6.3.2). Therefore, after the initial ~40 Å thick oxide film, growth under negative bias was stopped.

Initial growth under negative bias could be because of the reactive O^* and/or O_2^+ reacting with Si.

In contrast to -50 V bias growth results, growth rates for positive substrate bias were significantly higher (see Figure 6.3.2). At 0 V bias on substrate, growth rates were slow compared to +50 V bias but unlike -50 V bias case, growth did not stop completely. After 180 min of oxidation, the oxide thickness was ~430 Å for a +50 V bias and ~180 Å for a 0 V bias. Higher growth rates observed at positive bias suggest that the oxidation process was enhanced by the transport of negatively charged oxidizing species through the oxide layer to the Si-SiO_2 interface.

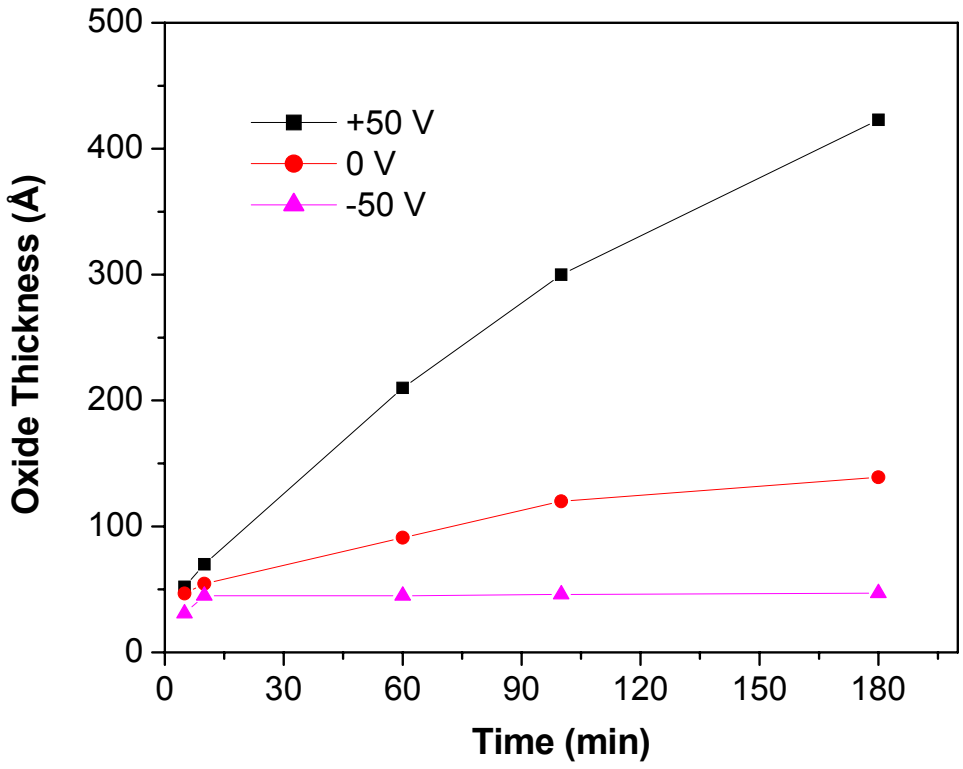


Figure 6.3.2 Oxide growth with time at +50, 0 and -50V DC bias applied on substrate holder

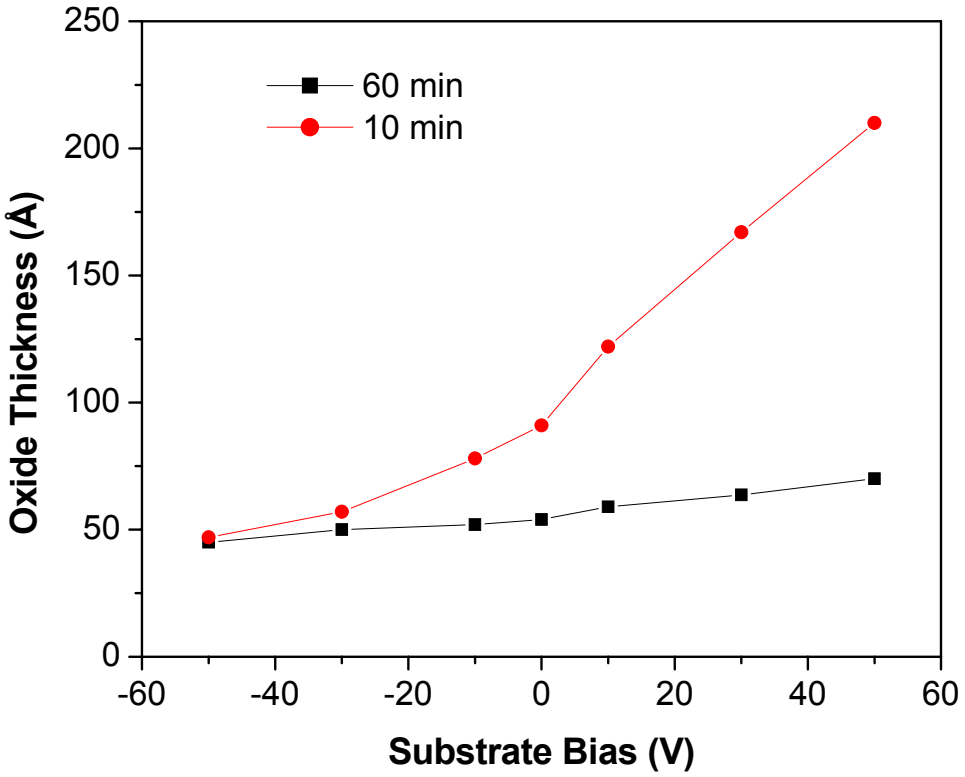


Figure 6.3.3: Oxide thickness after 10 min and 60 min for different substrate biases

6.3.1 Oxide Growth Mechanism

As discussed in section 3.3, ECR oxygen plasma contains the O_2, O_2^+ and O^* in the plasma. Electrons present at the SiO_2/plasma interface could react with reactive oxygen using the following reaction:

$$O + e \rightarrow O^- \ (E = -1.5 \text{ eV}) \quad \text{.....6.3.1.1}$$

Oxide growth from O_2 gas at the low temperature used during the experiments would be much less than the oxide thickness obtained. So we can rule out oxygen gas accountable for oxidation. After growing ~50 Å oxide layer, growth for -50 V bias stopped. Because of the very high negative bias, O^- formed at the oxide surface can not transport through the oxide layer; therefore oxidizing species responsible for initial oxide growth could be of O_2^+ and/or O^*. In case of +50 V bias, after first 5 min of oxidation, slightly higher oxide thicknesses was

obtained compared to -50 V or 0 V cases (Figure 6.3.2). Thus for thin oxide layer, applied DC bias or electric field did not significantly affect the oxide thickness. Therefore it is reasonable to assume that the O^*, which is not affected by the electric field, is responsible for growing thin oxide layers.

No growth for the large negative bias case signifies that O^* and O_2^+ are not the species responsible for thick ECR plasma oxide films (>40Å). Note that the reactive oxygen does not have any influence of electric field and if it was one of the species responsible for the growth, growth should have not stopped for the negative bias case. It was not possible for reactive oxygen to thermally diffuse through the oxide layer at the low temperatures used during the oxidation process to grow thick oxide layers.

High growth rates were observed as the bias was increased and this suggests that there is transport of negatively charged oxidizing species from SiO_2-plasma interface to Si-SiO_2 interface. O^- is larger than atomic O^*. If thermal diffusion of O^* is not possible (as seen in high negative bias case) at the temperatures used, it is certainly not possible for O^-. This implies that O^- was transported from the plasma-SiO_2 interface to the Si-SiO_2 interface under the influence of the electric field. While the exact transport mechanism for O^- to the Si-SiO_2 interface is still unknown, it is clear from our experiments that to grow thicker oxides, one needs negative ions transport through the oxide layer.

6.4 STRESSING RESULTS

N-channel MOSFET devices were stressed under DC bias and the change in threshold voltage and linear mobility was measured. The substrate current (I_{SUB}) was measured to optimize the stressing conditions. Current was measured while the gate voltage was varied for a fixed drain voltage [53].

An HP parameter analyzer was programmed to stress the n-channel. I_{DS}-V_{GS} and I_{DS}-V_{DS} data was recorded after time intervals of 10, 30, 100, 300, 1000, 3000, 10000, 30000 and 100000 seconds. MOSFET devices were fabricated as descried in chapter 4.

In the first experiment, as-grown ECR oxide was annealed at temperature 400, 500, 600, and 800^{o}C and n-MOSFET channel was tested for HCI degradation. As seen in Figure 6.4.1 and Figure 6.4.2, higher temperature annealing of as grown oxide helps in improving the channel resistance of ECR grown oxide. Annealing at 800^{o}C oxide showed best results.

In second experiment, following three types of gate oxides were fabricated and tested for the n-channel HCI degradation, as-grown ECR oxide (Sample-A), ECR oxide annealed at 800^{o}C prior to metallization (Sample-B, pre-PMA), Thermal oxide

All samples received post-metallization annealing in N_2 gas at 450^{o}C for 30 min at 1 atm. pressure. From Figures 6.4.3 and 6.4.4, ECR as-grown oxide showed much higher degradation compared to the oxide received 800^{o}C pre-PMA and the thermal oxide.

Due to the higher defect density, sample-B (pre-metallization annealing at 800^{o}C) initially showed faster degradation. Later its degradation properties became comparable to that of the thermal oxide. The defect density of the sample-B was only slightly lower than the sample-A, however sample-B's channel resistance to hot electron induces degradation was remarkably higher than that of sample-A. Higher degradation of as-grown oxide (sample-A) could be caused by the presence of many non-bridging O atoms and also due to strain in Si-O bonds. This is discussed in more detail in the next section.

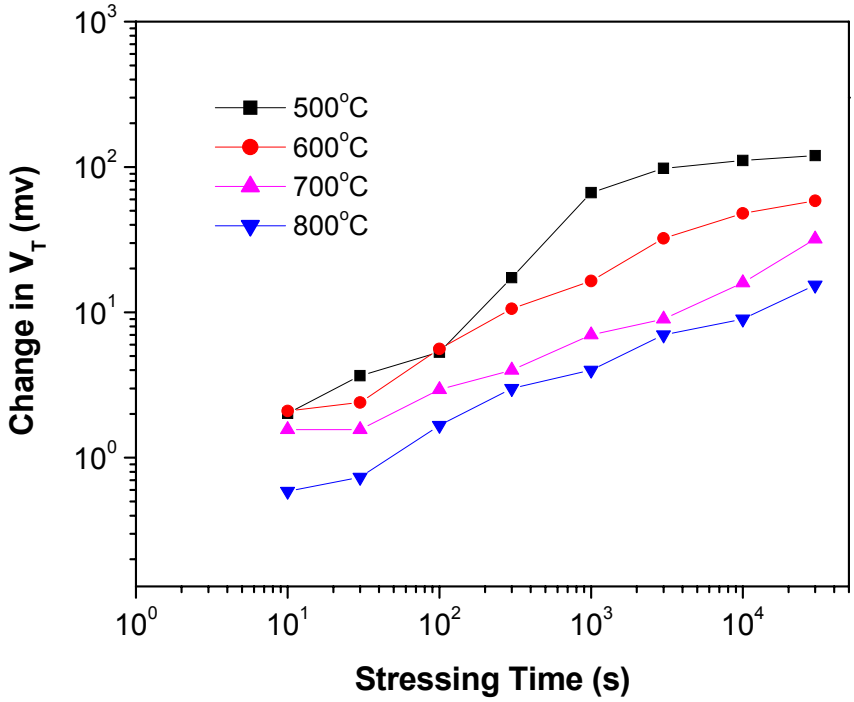


Figure 6.4.1 Change in threshold voltage with stressing time for different pre-metallization annealing temperature

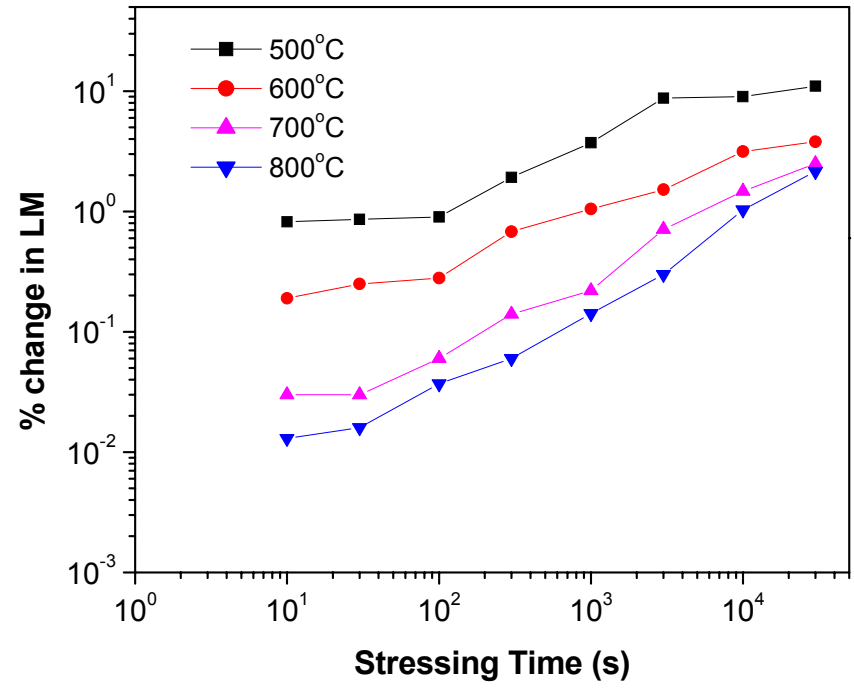


Figure 6.4.2 Change in linear mobility with stressing time at different pre-metallization annealing temperature

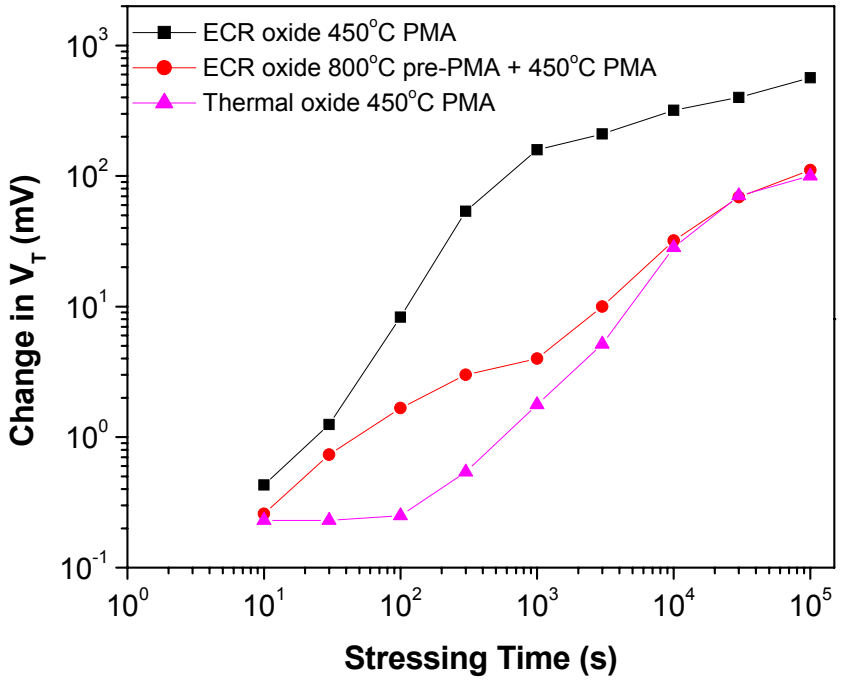


Figure 6.4.3 Change in threshold voltage with stressing time for different oxide samples

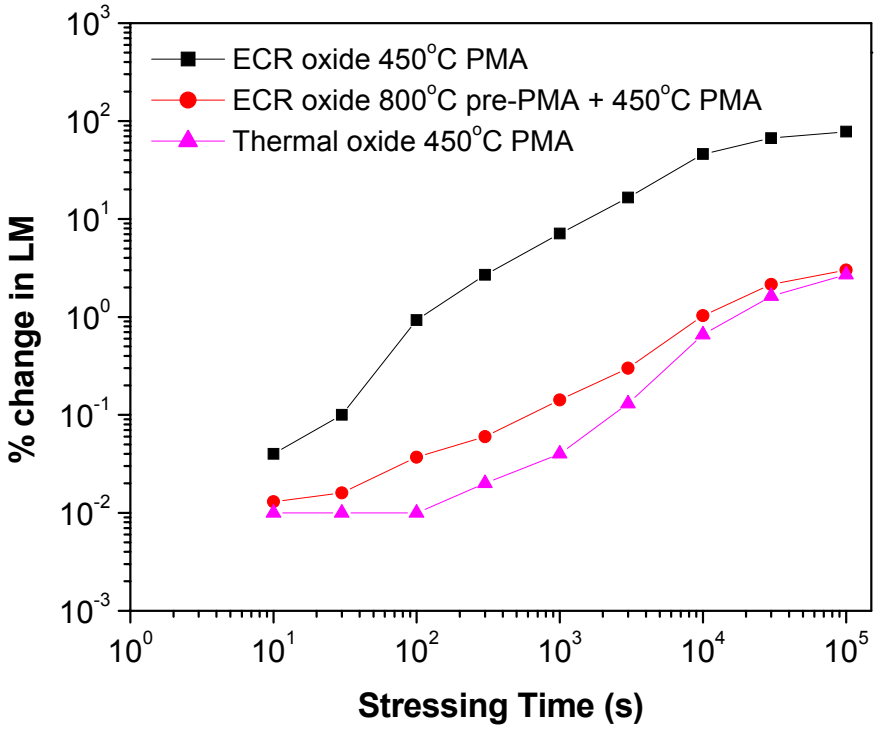


Figure 6.4.4: Change in linear mobility with stressing time for different oxide samples

6.5 FTIR STUDY OF PLASMA OXIDE FILMS

Studies from several groups have established that the IR absorption peak positions and half-widths of the absorption peaks change with the alteration in the physical properties of SiO_2, such as the level of strain present in the film [63]]. Kimura et al compared the IR absorption data on ECR oxides (grown at different temperatures) against thermal oxide. ECR oxides grown at low temperatures (<450^{o}C) were of low thickness. It was suspected that the shifting of the observed absorption peaks was due to the differences in oxide film thicknesses [8].

To eliminate the effect of thickness, we first measured the IR absorption of the as-grown ECR oxide, then annealed it for 30 min at 800^{o}C in N_2 gas, and then re-measured the same sample. The IR absorption of the as-grown and the annealed ECR oxides were compared to the thermal oxide (see Figure 6.5.1).

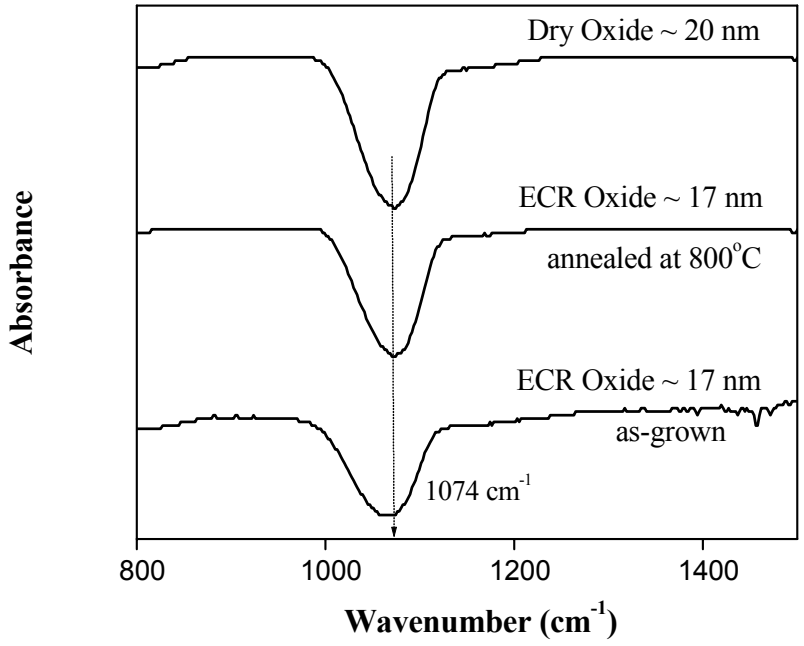


Figure 6.5.1 Infrared absorption spectrum of dry oxide and ECR oxide. Annealed ECR oxide and thermally grown dry oxide both have Si-O absorption peak at ~1074 cm^{-1}. As-grown ECR oxide has larger half-width and peak is shifted to ~1068 cm^{-1}.

The ECR plasma grown oxide, annealed at 800^{o}C, has the Si-O stretching absorption peak (1074 cm^{-1}) and the FWHM same as that of the thermally grown dry-oxide. In the as-grown ECR oxide, the Si-O stretching absorption peak is shifted to a lower wavenumber ~1068 cm^{-1} (red shift). It also has a broader half-width when compared to the annealed ECR oxide. This shift to a lower wavenumber can be elucidated by the following expression [20]:

$$v^2 = (k / m_o)\left[\sin^2(\theta / 2)\right] \quad \text{.....6.5.1}$$

Where v is wavenumber, k is force constant (inversely varying with Si-O bond length), and θ is the Si-O-Si bond angle (~144^{o}) in amorphous SiO_2 [20]. A lower v for the as-grown ECR oxide could be because of the longer Si-O bond or due to a change in the bond angle.

The as-grown ECR oxide Si-O stretching absorption peak has a lower intensity compared to the annealed ECR oxide. This intensity is directly related to the number of Si-O bonds that exist in the oxide. We speculate that there are many nonbridging O atoms present in the as-grown ECR oxide. During annealing many of these O atoms bridge with neighboring Si atom to form Si-O bond and this results in the higher intensity for the annealed samples.

The discussion above indicates that the low temperatures ECR plasma oxide films were of inferior quality. Due to the low temperatures used during the film formation and the plasma oxidation reaction mechanism, atoms may have not arranged themselves in the lowest energy configuration. Thus many nonbridging O atoms are present. Annealing the ECR oxide at a higher temperature might have allowed atoms to rearrange themselves in the minimum energy configuration and thus made the ECR oxide physically indistinguishable from the thermal dry-oxide.

6.6 GROWTH RATE DEPENDENCE ON Si WAFER ORIENTATION

The growth rate of the silicon dioxide depends on the Si wafer orientation [58]. The rate of oxidation is higher for the orientation having more Si atoms present at the surface. Below is the order of the oxidation rate in the linear region of oxidation:

$$(110) > (111) > (100)$$

N-type (111) and (100) orientated wafers were used to determine the orientation dependent growth rate for ECR plasma oxidation. To ensure the exact plasma conditions during oxidation both (111) and (100) orientations were loaded together into the reactor chamber. Figure 6.6.1 shows that the plasma oxidation growth rate is not dependent on the orientation of Si wafer. This is very useful for the applications where the thin oxide film needs to be grown on slanted surfaces. Note, a slanted surface could have many different orientations. One such example is the growth of liner oxide in shallow trench isolation (STI) used for separating devices in a typical CMOS process [56]. As discussed above, different orientations would result in different oxide thicknesses. This leads to the faceting effect at the bottom and creates serious challenge for the device reliability [56]. Use of ECR plasma grown liner oxide can help in eliminating such issues related to orientation dependent oxide growth.

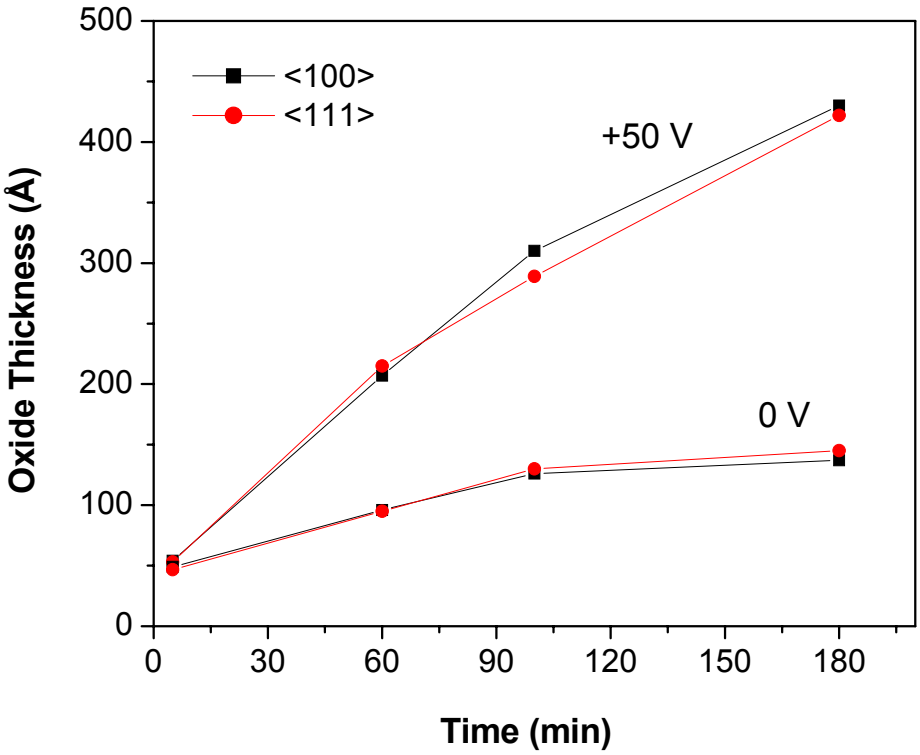


Figure 6.6.1: ECR plasma oxide thickness with time for wafers orientation (111) and (100) at +50 V and 0 V DC bias cases. Unlike the thermal oxidation case, Oxide growth rates for both the orientation were similar

6.7 EFFECT OF FLUORINE GAS ON ECR OXIDE

As discussed in earlier (see section 2.5) that the presence of fluorine gas during the thermal oxidation process increases the oxidation rate [23]. The fluorine incorporated thermal oxides have been investigated and shown to reduce the mechanical stress of the oxide film and improve the gate oxide electrical properties [24], [61].

Fluorine inclusion in the oxide has been also tried during the plasma oxidation of Si [25-30]. In plasma oxidation of Si, presence of fluorine was found to increase the growth rate [24] and at the same time reduce the interface defect density [27] by on order of magnitude. After reviewing these results, we also decided to see the effect of fluorine of oxide growth rate and most importantly on the reliability of the MOSFET device channel against the hot carrier induced degradation.

6.7.1 Growth Results

For these runs, 5% F_2/He and 10% O_2/He gas mixtures were used in the plasma chamber. A 150 W of microwave power was supplied to the chamber. Figure 6.7.1 compares the oxide growth rates using O_2/He gas with and without fluorine gas in the plasma. Inclusion of fluorine gas in the plasma has substantially increased the oxide growth rate. Using O_2/He gas only ~130 Å of oxide was grown in 60 min. The plasma oxidation was carried out at 100^{o}C temperature and 5 mT chamber pressure. For the same conditions, fluorine assisted oxide growth resulted in a ~1500 Å thick oxide film. Fluorine is suspected to open up the oxide network to enhance diffusion. Fluorine also breaks the Si-Si bonds at Si wafer more aggressively and provides more Si dangling bonds for oxidizing species. The exact mechanism is still not understood.

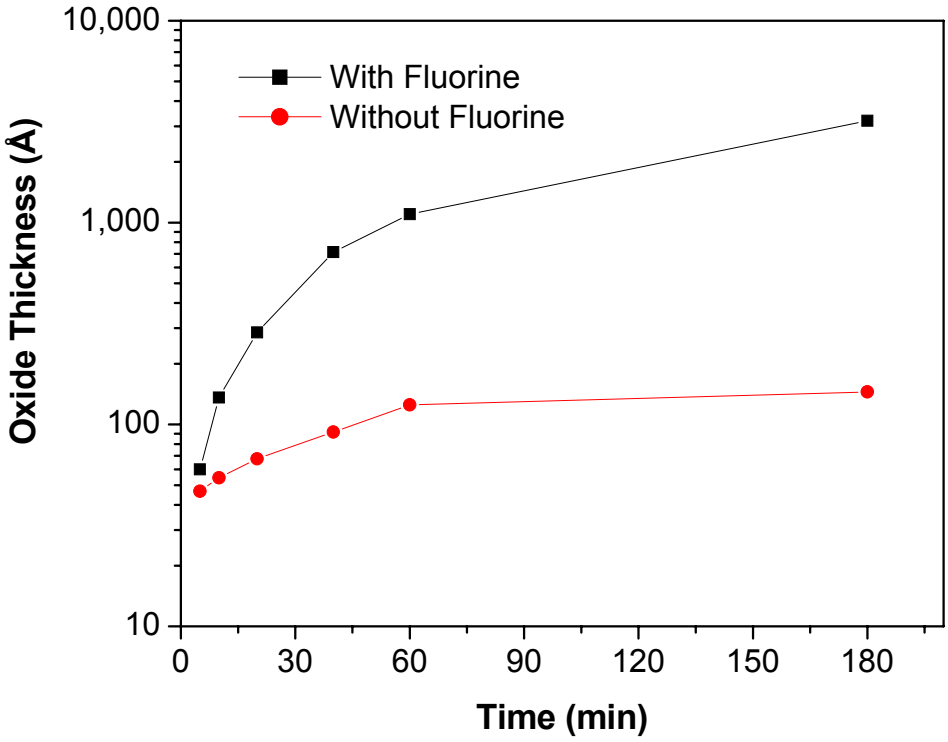


Figure 6.7.1: Increase in growth rate is more than ~15 times.

6.7.2 Effect of Chamber Pressure

Figure 6.7.2 shows the effect of pressure on oxide growth rate. In our reactor the minimum pressure with the given gas flow rates was 3 mT. We observed a decrease in thickness at higher pressures. At high pressures, the density of oxidizing species decreases and this could be the cause of the low oxide growth rates obtained at high pressure.

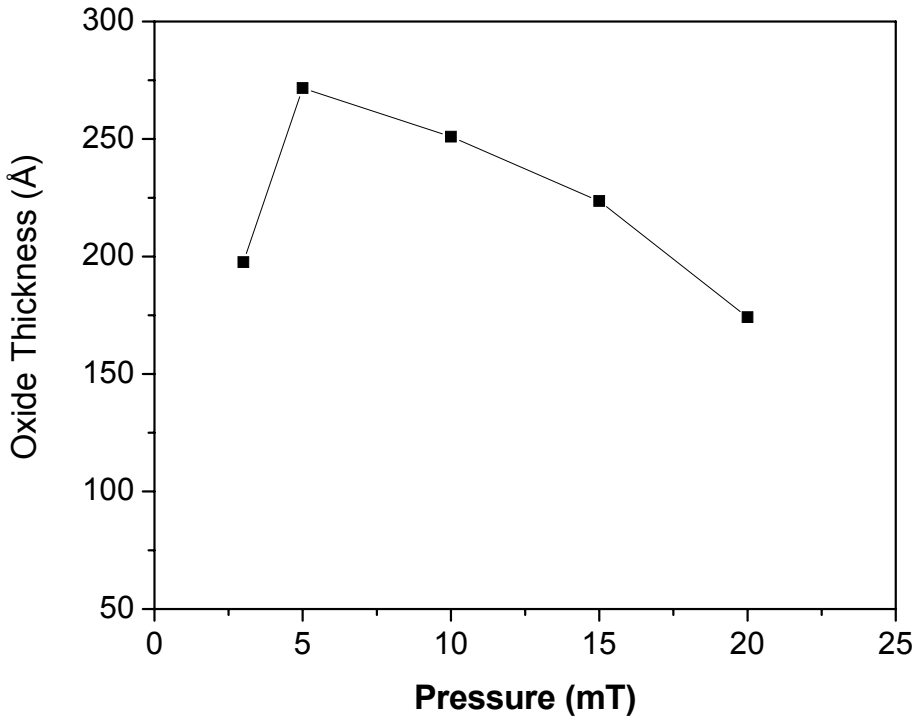


Figure 6.7.2: Effect of pressure on oxide growth for runs with fluorine.

6.7.3 Effect of Temperature

High oxide growth rates were observed even at low temperatures. At 300^{o}C there was an increase in the oxide thickness but at higher temperatures ~500^{o}C, thickness dropped. This decrease in thickness could be due to simultaneous etching of the growing silicon dioxide layer. Fluorine has been used to etch silicon dioxide and it forms volatile SiF_4 as a by-product. Considering the limited scope of the project we did not go any further to investigate the reason behind this.

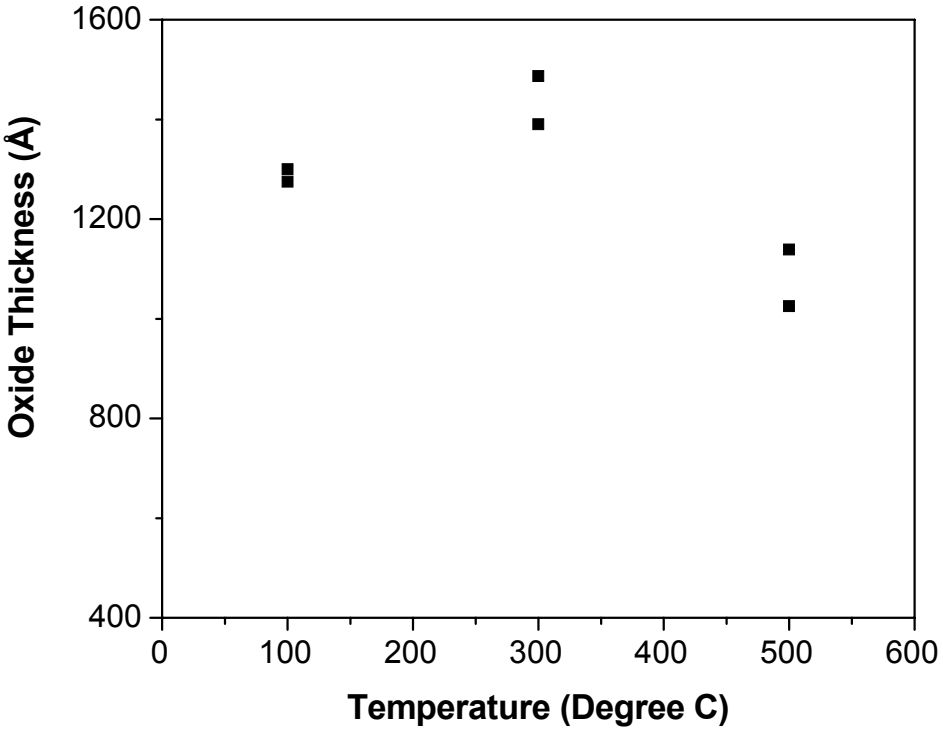


Figure 6.7.3: Effect of temperature on oxide growth rate. Pressure 5 mT, power 150 W, 20 min, 5% F_2/He 1 sccm, 10% O_2/He 20 sccm.

6.7.4 Effect of Gas Flow Rate

The gas flow rate of 5% F_2/He was increased from 1 sccm to 5 sccm while maintaining the 10% O_2/He gas flow rate to 20 sccm. Chamber pressure was maintained at 5 mT. This led to the increase in F_2/O_2 ratio from ~2.5% to ~12%. As shown in Figure 6.7.4, oxide thickness increased until the ratio of F_2/O_2 reached 8%. For higher fluorine content (>8% F_2/O_2) in the plasma gaseous mixture, thickness was found to decrease. The decrease in the oxide thickness at high F_2/O_2 ratios could be attributed to the etching effect of fluorine.

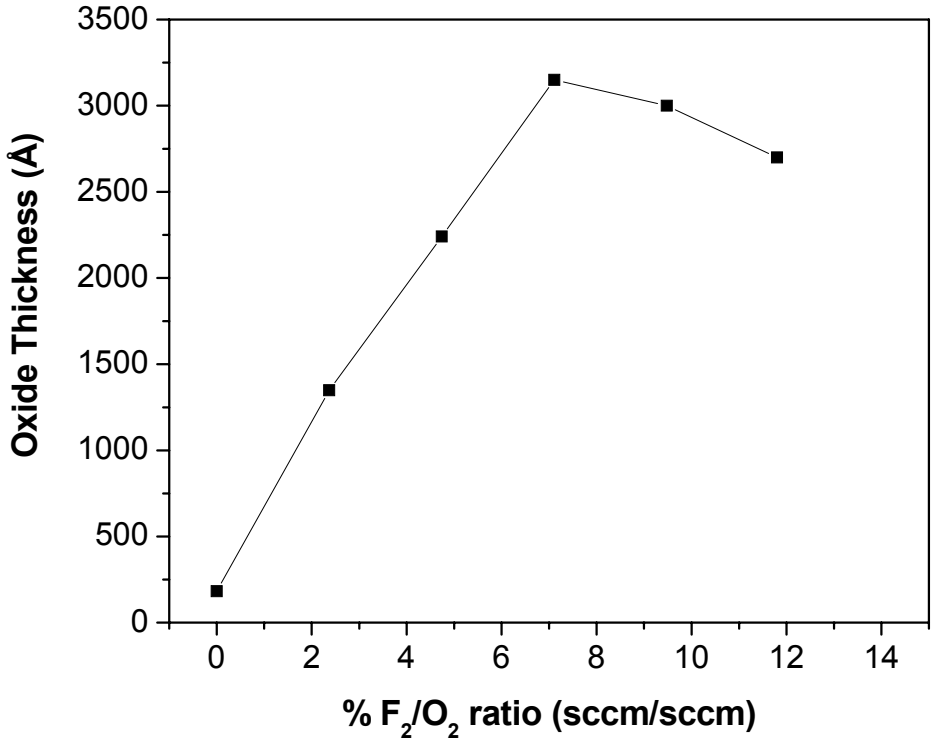


Figure 6.7.4 Growth rate increased as fluorine to oxygen ratio was increased.

6.8 FLUORINE INCORPORATED GATE OXIDE RELIABILITY

Figures 6.8.1 and 6.8.2 show the hot electron induced (HEI) channel degradation of an NMOS device. Change in threshold voltage and linear mobility of electrons in the channel are plotted against the stressing time. The results from thermal oxide, ECR plasma oxide, and fluorine incorporated ECR plasma oxide are compared. ECR grown gate oxide with no fluorine was found to degrade ~100 times faster than thermal oxide. Whereas fluorine incorporated oxide showed resistance against HEI degradation similar to that of thermal oxide. Si-F bonds formed at the Si-SiO_2 interface reduced the defect density. Fluorine not only effectively passivates surface dangling bonds, but also provides a much stronger Si-F bond to enhance the reliability of plasma grown gate oxides. Therefore the inclusion of fluorine in the oxide improved the channel resistance against hot electron induced degradation.

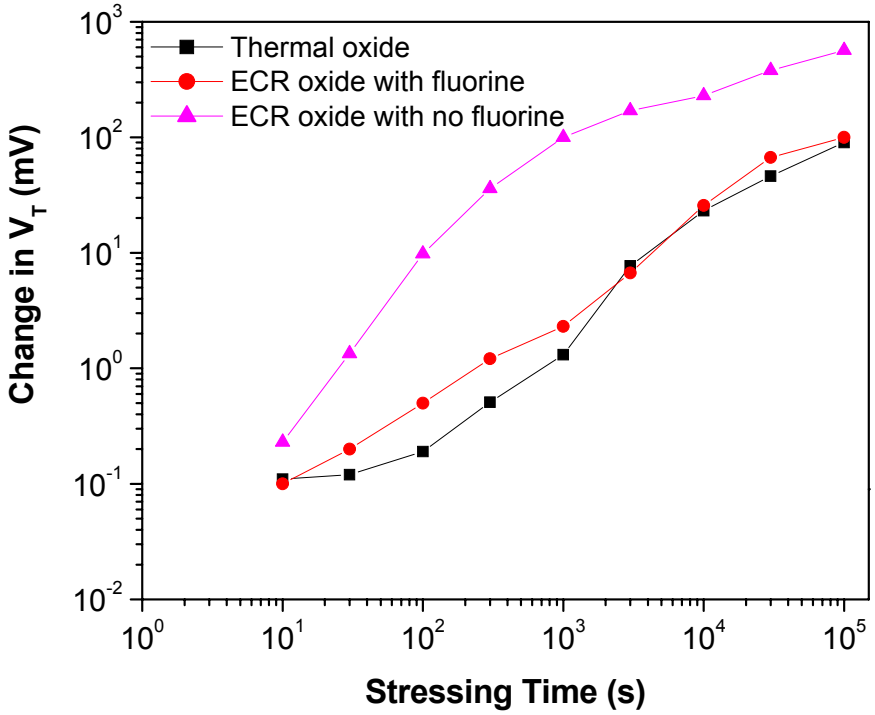


Figure 6.8.1: ECR oxide with no fluorine degraded very fast compared to thermally grown gate oxide. Fluorine incorporated ECR oxide showed similar channel degradation properties similar to thermally grown oxide.

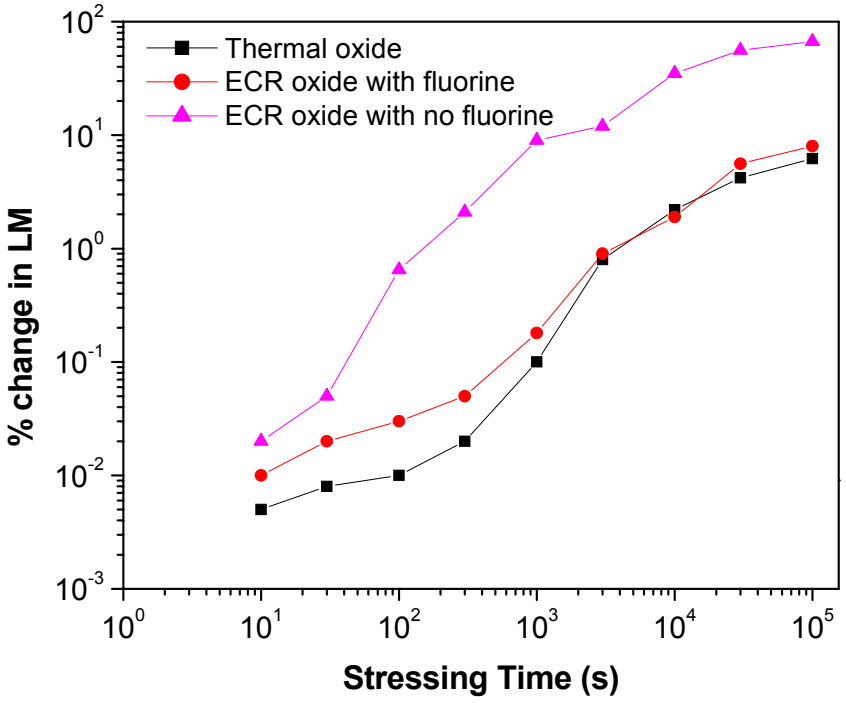


Figure 6.8.2: Change in linear mobility and threshold voltage with stressing time.

6.9 CHEMICAL COMPOSITION ANALYSIS

Depth profile analysis using XPS shows that the O to Si ratio is ~2 in our samples. FTIR analysis confirmed the presence of Si-O bonds in our ECR oxide samples. Combining results from XPS (A_O/A_{Si} ~2) and FTIR (presence of Si-O bonds), we conclude that SiO_2 was grown by the plasma oxidation of Si. Also samples grown with fluorine in the plasma had only ~1-2% of fluorine present uniformly through out oxide thickness.

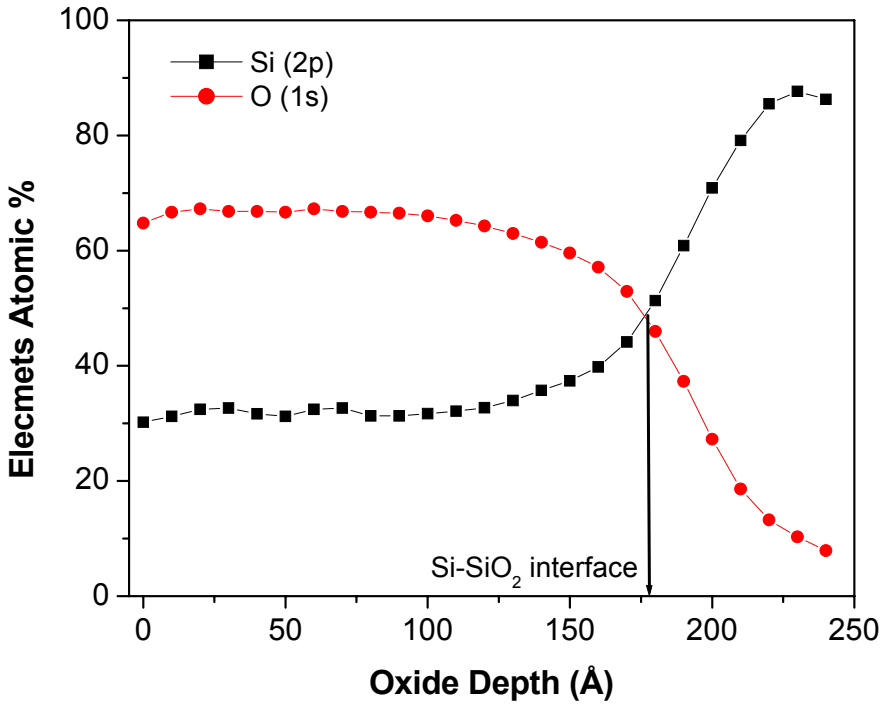


Figure 6.9.1: XPS depth profiling of oxide film.

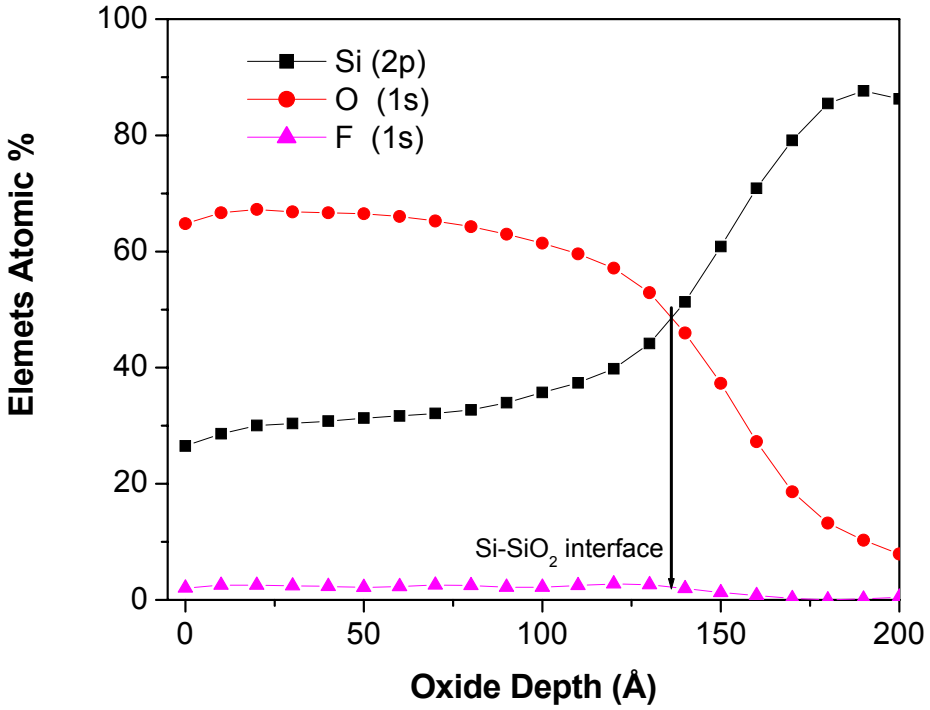


Figure 6.9.2: XPS depth profiling of oxide film reveals ~1% fluorine in the oxide with ~2.5% F_2/O_2 ratio.

6.10 MOSFET DEVICE PARAMETERS

Theoretical values of mobility, for the boron doping density levels 2 x 10^{17}-7 x 10^{17} cm^{-3}, are in the range of 420-320 cm^2/V.s. As seen in the graph below, thermally-grown oxide, annealed ECR oxide, and fluorinated oxide mobility are in the same range. Also as expected, there was a one to one correlation between mobility and defect density at the Si-SiO_2 interface. For higher defect densities lower mobility was found.

	Thermal oxide	**ECR oxide (annealed 450°C N_2)**	**ECR oxide w/F (annealed 450°C N_2)**
Interface Defect Density (D_{it})	3 x 10^{10} $cm^{-2}eV^{-1}$	1 x 10^{11} $cm^{-2}eV^{-1}$	3 x 10^{10} $cm^{-2}eV^{-1}$
Oxide Breakdown Strength (E_{BR})	10-12 MV/cm	8-11 MV/cm	8-11 MV/cm
Mobility	410 cm^2/V.s	350 cm^2/V.s	380 cm^2/V.s

Table 6.10.1: Comparison of MOS and MOSFET device parameters for thermal oxide, ECR oxide and fluorine incorporated ECR oxide.

CHAPTER 7. CONCLUSIONS

We have successfully developed a reliable gate oxide for a MOSFET at low temperature using ECR plasma. We have systematically studied the ECR plasma properties by using OES and Langmuir probe. After learning the effect of temperature, pressure, and DC bias on oxide growth, we fabricated MOS capacitors to study the effects of process variables on the interface defect density. The addition of fluorine in the plasma gaseous mixture was found to considerably increase the oxide growth rate, reduce the defect density and improve stability of the device. The significant results are as follows:

7.1 PLASMA CHARACTERIZATION

Optical emission spectroscopy (OES) was used to identify the reactive species present in the ECR plasma of oxygen. Characteristic peaks for O_2^+ ions and reactive oxygen (O^*) were observed in the plasma. No other ions or reactive species e.g. H or OH were present in the plasma. Plasma with fluorine gas had characteristic peaks for reactive fluorine (F^*) at 685.6 and 703.7 nm.

Using the data obtained from the Langmuir probe measurement we established that the oxygen plasma sheath potential was ~6 V. Lower plasma potential reduces the damage to the film due to the ion bombardment. Plasma density was calculated as ~ $3x10^{10}$ cm^{-3}, which is relatively low compared to literature quoted values for ECR plasma (~ $1x10^{12}$ cm^{-3}). The use of low microwave power (~150 W), higher minimum pressures (~1 mT), and low magnetic field strength (~150 G) near the Langmuir probe region were the main reasons for low plasma density.

7.2 ORIENTATION DEPENDENCE

The oxide grown on Si wafers with <111> and <100> orientations had similar oxide thickness. This result is quite different from the thermal oxidation case where in the linear region of oxide growth, growth is proportional to the number of Si atoms present at the surface. In case of thermal oxidation, <111> orientation has a ~1.68 times higher oxide growth rate than the <100> orientation. In the case of plasma oxide, the linear region ends at a thickness of ~40 Å and the reaction becomes transport controlled. Where we do not observe faster growth rates for Si having more Si atoms present at the surface.

7.3 STRUCTURAL AND ELEMENTAL ANALYSIS

The FTIR study confirms the presence of an Si-O bond in our plasma grown films. The Si-O stretching absorption peak for as-grown ECR samples were low in intensity, signifying the presence on many nonbridging O atoms in the oxide. The peak was shifted to a lower wavenumber and had a higher FWHM compared to the same sample annealed at a much higher temperature. Fluorine incorporated oxide films did not show any Si-F or O-F peaks. This was due to very low fluorine percentage (~1%) in our samples, which was below the detection limits of FTIR.

Elements present in the plasma film were identified using XPS. In ECR plasma oxide films, XPS analysis showed that the atomic concentration ratio of O/Si is ~2. Fluorine incorporated oxide films had ~1-2% fluorine atomic concentration uniformly present in the oxide film. Higher concentrations were found for higher fluorine partial pressures in the plasma chamber.

7.3 GROWTH RESULTS AND MECHANISM

Silicon dioxide films were grown by direct oxidation of silicon wafers using an ECR plasma of pure oxygen gas. From the OES study we found that concentrations of reactive oxygen and O_2^+ ions were high at low pressures (1 mT). Consequently, we observed a thicker oxide film at lower pressures.

Growth rate was virtually independent of temperature. Oxide grown at 100-500^{o}C temperatures did not show any significant difference in oxide growth rate. Activation energy measured was ~0.02 eV compared to ~1.2 eV for thermal oxide. This implies that the reactions were plasma enhanced.

Higher growth rates were obtained when the substrate was positively biased. A negative biasing resulted in the slower oxide growth and at a bias of –50 V dc we could only grow 50 Å, even after 3 hrs of oxidation time. Initial oxide growth (up to 40 Å) was because of some or all of the O_2^+, O^* and O^- ions. Growth in thick oxide films (t >50 Å) was limited by transport for the oxidizing species (O^-). Transport of oxidizing species was electric field assisted.

Presence of fluorine in the plasma gas mixture was found to substantially increase the growth rate, by more than ~15 times. Reason for such an enhanced growth is still unknown. It is believed that the F^*, which is highly reactive, increases the growth rate by one or both of the following mechanisms.

i. It easily breaks the Si-Si bonds at Si-SiO_2 interface and the Si dangling bond is now free to react with the oxidizing species.

ii. It opens up the oxide network and thus increases the diffusion of oxidizing species through the oxide layer.

7.4 MOSFET DEVICE FABRICATION AND ELECTRICAL CHARACTERIZATION

MOS capacitors and MOSFET devices were fabricated using Al as a gate metal. Annealing in a N_2 gas at 450^{o}C was found to reduce the defect density by more than an order of magnitude. It was found that an ECR oxide grown with a pure oxygen plasma had a D_{it} of ~1x10^{11} cm^{-2}eV^{-1} and an oxide breakdown strength of ~8-11 MV/cm. However, fluorine incorporated oxide, containing ~1.0-2.0 % fluorine, had a defect density of ~3x10^{10} cm^{-2}eV^{-1}, which is equivalent to the values obtained for the thermal oxide.

7.5 RELIABILITY OF MOSFET DEVICE

We have successfully fabricated MOSFET devices using an ECR plasma grown oxide as the gate oxide. We have also studied the reliability of an ECR grown gate oxide and compared it to a dry-oxide thermally grown at much higher temperatures. We found that the as-grown ECR oxide shows higher hot carrier induced degradation. It was approximately 2 orders of magnitude higher compared to thermal gate oxide. Annealing at higher temperatures, ~800^{o}C, improved the channel resistance for the HCI degradation and its device lifetime became comparable to devices with thermally grown gate oxide. Later we fabricated devices with low temperature fluorine incorporated ECR oxide, which showed a channel resistance to hot electron induced degradation comparable to that of thermally grown dry-oxide.

CHAPTER 8. FUTURE WORK

1. On a flat Si wafers we have shown using <100> and <111> oriented wafers that oxide growth using oxygen plasma is independent of orientation. We pointed out that one of the possible uses of this would be in Shallow Trench Isolation (STI) structures where on slanted surface many other orientations are also present. It would be interesting to see the oxide growth results on an actual STI structure.

2. It is still not fundamentally clear which gas species is responsible for growing the thin oxide layer. By changing the plasma parameters and, observing the change in reactive species and oxide growth rates, one may be able to actually point out the species responsible for growing the thin oxide layer. This would require an in-situ Ellipsometer to measure the oxide thickness with time.

3. We always assumed the refractive index (n) of oxide film was ~1.46. Using an Ellipsometer that could independently provide the thickness and refractive index would give an exact value of refractive index and much more precise thickness measurements.

4. We have observed significantly higher oxide growth rates using a fluorine gas in the plasma. It was suggested that this could be due to the opening of the oxide network and also aggressively breaking of Si bonds by reactive fluorine at the Si-SiO_2 interface. A study to actually see how this process is really happening would be interesting.

5. For thin film transistors (TFTs) on plastic substrates you need low temperature oxide growth processes. Currently oxide is deposited using plasma enhanced chemical vapor deposition (PECVD). Alternatively one could also deposit Si using PECVD and then try to oxidize it using plasma oxidation technique.

6. One could also try to first make silicon nitride using a N_2 plasma and then deposit silicon dioxide. This structure would have a higher dielectric constant, which is required in current CMOS processing.

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